PENG LI

Professor
Department of Electrical and Computer Engineering
Texas A&M University

Member of Faculty of Neuroscience
Texas A&M University

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EDUCATION

Ph.D.	Carnegie Mellon University, Electrical & Computer Engineering, 2003
Master's	Xi'an Jiaotong University, Systems Engineering, 1997
Bachelor's	Xi'an Jiaotong University, Information Science & Engineering, 1994

APPOINTMENTS & EXPERIENCES

Professor
Department of Electrical and Computer Engineering, Texas A&M University
September 2015 – Present

Associate Professor
Department of Electrical and Computer Engineering, Texas A&M University
September 2010 – August 2015

Graduate Faculty
School of Graduate Studies, Texas A&M Health Science Center
June 2011 – Present

Faculty
Texas A&M Institute for Neuroscience
February 2011 – Present

Assistant Professor
Department of Electrical and Computer Engineering, Texas A&M University
August 2004 – August 2010

Postdoctoral Research Fellow
Department of Electrical and Computer Engineering, Carnegie Mellon University
December 2003 – July 2004

Graduate Intern Researcher
IBM Austin Research Laboratories
Summer 2002

RESEARCH INTERESTS

Integrated Circuits and Systems, Brain Inspired Computing, Electronic Design Automation, and Computational Brain Modeling

Current Topics:

- Brain-inspired learning algorithms, circuits, and architectures
- Spiking neural networks and spike-dependent learning mechanisms
- IC power delivery, voltage regulation/conversion, and power management
- Modeling, optimization & verification of analog/mixed-signal circuits and systems
- Applied statistical learning and its applications to hardware system design
- Hardware machine learning accelerators
- Biophysically-plausible brain modeling and simulation
- Robust and verifiable machine learning

HONORS AND AWARDS

- **Best Paper Award**
  53rd IEEE/ACM Design Automation Conference (DAC), June 2016
  (Only three other individuals in the 54-year history of DAC have been recognized with four best paper awards)
- **ISCAS Honorary Mention Best Paper Award**
  The Neural Systems and Applications Technical Committee of IEEE Circuits and Systems (CAS) Society at IEEE International Symposium on Circuits and Systems (ISCAS)
  May 2016
- **Fellow of the IEEE**, Elected in Nov. 2015
- **William and Montine P. Head Fellow**
  College of Engineering, Texas A&M University, 2013-2014
- **Best Paper Hat Trick Award**
  50th IEEE/ACM Design Automation Conference (DAC), June 2013
  (for receiving the DAC best paper award three times)
- **DAC Prolific Author Award**
  50th IEEE/ACM Design Automation Conference (DAC), June 2013
- **DAC Top 10 Author in Fifth Decade**
  50th IEEE/ACM Design Automation Conference (DAC), June 2013
- **IEEE/ACM William J. McCalla ICCAD Best Paper Award**
  IEEE/ACM International Conference on Computer-Aided Design (ICCAD), November 2012
- **TEES Fellow Award**
  College of Engineering, Texas A&M University, 2011-2012
- **Best Paper Award**
  48th IEEE/ACM Design Automation Conference (DAC), June 2011

- Best in Session Award
  Semiconductor Research Corporation Techcon Conference, September 2009
- **NSF CAREER Award**
  National Science Foundation, 2008
- **Outstanding Professor Award**
  Department of ECE, Texas A&M University, December 2008
- **Best Paper Award**
  45th IEEE/ACM Design Automation Conference (DAC), June 2008
- **Inventor Recognition Award**
  Microelectronics Advanced Research Corporation, 2007
- **Inventor Recognition Award**
  Microelectronics Advanced Research Corporation, January 2006
- **Inventor Recognition Award**
  Semiconductor Research Corporation (SRC), November 2004
- **Best Paper Award**
  40th IEEE/ACM Design Automation Conference (DAC), June 2003
- **Inventor Recognition Award**
  Semiconductor Research Corporation (SRC), January 2001
- Best Paper Award Nominations

  IEEE/ACM ICCAD, one in 2006, two in 2008, one in 2018

TEACHING

Department of Electrical and Computer Engineering, Texas A&M University

- ECEN 714 Digital Integrated Circuit Design, Fall 2018
- ECEN 454 Digital Integrated Circuit Design, Fall 2018
- ECEN 751 Advanced Computational Methods for Integrated System Design, Fall 2018
- ECEN 689-601: VLSI Machine Learning Systems, Spring 2018
- ECEN 248 Introduction to Digital Systems Design, Fall 2017
- ECEN 751 Advanced Computational Methods for Integrated System Design, Spring 2017
- ECEN 714 Digital Integrated Circuit Design, Fall 2016
- ECEN 454 Digital Integrated Circuit Design, Fall 2016
- ECEN 751 Advanced Computational Methods for Integrated System Design, Spring 2016
- ECEN 714 Digital Integrated Circuit Design, Fall 2015
- ECEN 454 Digital Integrated Circuit Design, Fall 2015
- ECEN 751 Advanced Computational Methods for Integrated System Design, Spring 2015

- ECEN 454 Digital Integrated Circuit Design, Fall 2014
- ECEN 454 Digital Integrated Circuit Design, Spring 2014
- ECEN 751 Advanced Computational Methods for Integrated System Design, Spring 2014
- ECEN 454 Digital Integrated Circuit Design, Fall 2013
- ECEN 689-603 Advanced Computational Methods for Integrated System Design, Spring 2013
- ECEN 454 Digital Integrated Circuit Design, Fall 2012
- ECEN 454 Digital Integrated Circuit Design, Spring 2012
- ECEN 689-608 Advanced Computational Methods for Integrated System Design, Spring 2012
- ECEN 449 Microprocessor System Design, Fall 2011
- ECEN 689-608 Advanced Computational Methods for Integrated System Design, Spring 2011
- ECEN 454 Digital Integrated Circuit Design, Fall 2010
- ECEN 681-644 Computer Engineering Seminar, Fall 2010
- ECEN 689-604 Emerging VLSI CAD Applications and Techniques, Spring 2010.
- ECEN 681-648 Computer Engineering Seminar, Spring 2010,
- ECEN 454 Digital Integrated Circuit Design, Fall 2009
- ECEN 681-644 Computer Engineering Seminar, Fall 2009
- ECEN 689-606 Emerging VLSI CAD Applications and Techniques, Spring 2009
- ECEN 468 Advanced Logic Design, Fall 2008
- ECEN 689-618 Introduction to CAD for Digital & Analog VLSI and Its Parallel Implementation, Spring 2008
- ECEN 475 Introduction to VLSI System Design, Spring 2008
- ECEN 475 Introduction to VLSI System Design, Fall 2007
- ELEN 454 Digital Integrated Circuit Design, Spring 2007
- ELEN 689 Advanced Integrated Circuits Analysis, Fall 2006
- ELEN 454 Digital Integrated Circuit Design, Fall 2006
- ELEN 689 Advanced Integrated Circuits Analysis, Spring 2006
- ELEN 454 Digital Integrated Circuit Design, Fall 2005
- ELEN 454 Digital Integrated Circuit Design, Spring 2005
- ELEN 689610 Computer-Aided Simulation and Modeling of VLSI Circuits, Fall 2004

Research grants

Active

Project 26:	Enabling Adaptive Voltage Regulation: Control, Machine Learning, and Circuit Design
Sponsor:	NSF
PI:	Peng Li
Co-PI:	Edgar Sanchez-Sinencio
Amount:	$360,000 (total)
Period:	8/1/2018 – 7/31/2021

Project 25:	BIGDATA: IA: Collaborative Research: From Bytes to Watts - A Data Science Solution to Improve Wind Energy Reliability and Operation
Sponsor:	NSF
PIs:	TAMU: Yu Ding (PI), Peng Li (Co-PI) and Bani K. Mallick (Co-PI); U. Michigan: Eunshin Byon (PI); U. Connecticut: Jiong Tang (PI)
Amount:	$1,299,797
Period:	10/1/2017 – 9/30/2020

Project 24:	Hierarchical Analog and Mixed-Signal Verification Using Hybrid Formal and Machine Learning Techniques
Sponsor:	Semiconductor Research Corporation (SRC)
PI:	Peng Li
Amount:	$246,000
Period:	11/1/2016 – 10/31/2019

Project 23:	E2CDA: Type II: Self-Adaptive Reservoir Computing with Spiking Neurons: Learning Algorithms and Processor Architectures
Sponsor:	NSF and Semiconductor Research Corporation (SRC)
PI:	Peng Li
Amounts:	$499,113
Period:	10/1/2016 – 9/30/2019

Project 22:	Design of Energy-Efficient On-Chip Power Delivery: A System-Theoretic Approach
Sponsor:	Qatar National Research Fund (QNRF)
Lead PI:	Peng Li
Co-Lead PI:	Tingwei Huang (TAMU-Qatar)
Amounts:	Total: $702,320
Period:	6/1/2016 – 12/31/2019

Project 21:	Development and Assessment of Machine Learning based Analog and Mixed-Signal Verification
Sponsor:	Semiconductor Research Corporation (SRC)
PI:	Peng Li
Amount:	$255,000

Period: 1/1/2019 – 12/31/2021
Status: Tentatively awarded by the sponsor (final approval pending)

Pending

Project title: Knowledge-Driven and Verifiable Bayesian Learning under Data Shortfalls for Accelerated Material Discovery
Sponsor: DARPA
PIs: TAMU: PI: Zhangyang Wang, Co-PIs: Peng Li, Xiaoning Qian, Raymundo Arroyave
Columbia: Junfeng Yang
Amount: $968,739
Period: 12/07/2018 – 6/06/2020

Project title: SHF: Small: Hunting Rare Design Failures for Reliability-Critical Circuits – A Data Approach
Sponsor: NSF
PI: Peng Li
Amount: $492,363
Period: 10/1/2019 – 9/30/2022

Project title: Machine Learning Acceleration with 3D IC Architecture/Circuit Co-Design
Sponsor: Semiconductor Research Corporation (SRC)
PI: Sung-Kyu Lim (GaTech)
Co-PI: Peng Li (TAMU)
Amount: $360,000
Period: 1/1/2019 – 12/31/2021

Title: Machine Learning for Smart Grid Optimal Network Topology Control
Sponsor: Qatar National Research Fund (QNRF)
PIs: Garng M. Huang (TAMU-Qatar), Peng Li (TAMU-College Station)
Amount: $700,000
Period: 1/1/2019 – 12/31/2021

Completed

Project 20: Enabling Electronic Design using Data Intelligence
Sponsor: NSF - NSF Innovation Corps (I-Corps)
PI: Peng Li
Amount: $50,000
Period: 4/1/2017-9/30/2018

Project 19: Taming the Stability Challenge of Analog and Mixed-Signal Systems
Sponsor: NSF
PI: Peng Li
Co-PI: Edgar Sanchez-Sinencio
Amount: Total: $399,999 Peng Li: approximately 57%
Period: 8/1/2014 – 7/31/2018

Project 18:	Methods for Efficient Analysis of Analog ICs with Large Extracted Power Networks
Sponsor:	Intel Corporation
PI:	Peng Li
Amount:	$60,000
Period:	12/1/2015 – 11/31/2016

Project 17:	Statistical Analog Design Property Checking
Sponsors:	Semiconductor Research Corporation (SRC/GRC) & Texas Analog Center of Excellence (TxACE)
PI:	Peng Li
Amount:	$240,000
Period:	8/1/2013 – 7/31/2016

Project 16:	Analysis and Characterization of Switched-Mode DC-DC Power Converters
Sponsors:	Semiconductor Research Corporation (SRC/GRC), Texas Instruments and Texas Analog Center of Excellence (TxACE)
PI:	Peng Li
Amount:	$165,000
Period:	2/1/2013 – 1/31/2016

Project 15:	Collaborative Research: Integrated Verification, Built-in Self-test and Tuning for Digitally-Intensive Analog Systems
Sponsor:	NSF
PIs:	Peng Li (lead) and Chris J. Myers (U. of Utah)
Amount	Total: $450K Peng Li: $225K
Period:	8/1/2011 – 7/31/2015

Project 14:	CAREER: Parallel CAD Algorithms on Emerging Multi-Core Platforms
Sponsor:	NSF
PI:	Peng Li
Amount:	$400,000
Period:	8/1/2008 – 7/31/2014

Project 13:	Hierarchical Model Checking for Practical Analog/Mixed-Signal Design Verification
Sponsors:	Semiconductor Research Corporation (SRC/GRC) & Texas Analog Center of Excellence (TxACE)
PI:	Peng Li
Amount:	$180,000
Period:	8/1/2010 – 1/31/2014

Project 12:	System-Level Models and Design of Power Delivery Networks with On-Chip Voltage Regulators
Sponsors:	Semiconductor Research Corporation (SRC/GRC), Texas Analog Center of Excellence (TxACE)
PI:	Peng Li
Amount:	$180,000

Period: 8/1/2010 – 1/31/2014

Project 11: Digital Neuromorphic Classifier Circuits
Sponsor: Semiconductor Research Corporation (SRC/GRC)
PI: Peng Li
Amount: $40,000 (gift)
Period: 10/1/2012-9/31/2013

Project 10: System-Theoretic Analysis and Design for Dynamic Stability of Memory Devices in Nanoscale CMOS and Beyond
Sponsor: NSF
PI: Peng Li
Co-PI: Garng M. Huang
Amount: $350,000 (total)
$175,000 (Peng Li)
Period: 8/1/2009 – 7/31/2013

Project 9: Thermal-Aware GPU-Based Design Engine for On-Chip Power Delivery in Power-Efficient Multi-Core Chips
Sponsor: NSF and Semiconductor Research Corporation (SRC)
PI: Peng Li
Amount: $344,985
Period: 8/1/2009 – 7/31/2013

Project 8: Multi-Core and Distributed Parallel Simulation for Design & Verification of Custom Digital and Analog ICs
Sponsors: Semiconductor Research Corporation (SRC/GRC) & Texas Analog Center of Excellence (TxACE)
PI: Peng Li
Amount: $300,000
Period: 8/1/2008 – 10/31/2011

Project 7: Models and Analyses for 3D IC Integrity & Digitally Intensive in Situ Test and Adaptation
Sponsor: Center for Circuit and System Solutions (C2S2), SRC Focus Center Research Program (FCRP)
PI: Peng Li
Amount: $100,000
Period: 11/1/2009 – 3/31/2011

Project 6: Automatic Stability Checking for Linear Analog Integrated Circuits
Sponsor: Texas Instruments
PI: Peng Li
Amount: $50,000 for one year
Period: 9/1/2009 – 11/30/2010

Project 5: Achieving Feasible Large-Scale Parametric Variation Analysis for Design & Test of Analog Systems in Advanced Technologies

Sponsor:	Center for Circuit and System Solutions (C2S2), SRC Focus Center Research Program (FCRP)
PI:	Peng Li
Amount:	$214,684
Period:	9/1/2006 – 10/31/2009

Project 4:	Automatic Model Generation and Optimization of Massively I/O Coupled Networks
Sponsors:	Semiconductor Research Corporation (SRC/GRC)/Freescale Semiconductor
PI:	Peng Li
Co-PI:	Jiang Hu
Amount:	$180,000 (total) $120,000 (Peng Li)
Period:	7/1/2006 – 9/30/2009

Project 3:	Advanced Parameterized Current Source Based Cell Characterization
Sponsor:	Intel Corporation (gift)
PI:	Peng Li
Amount:	$25,000
Period:	9/1/2007 – 8/31/2008

Project 2:	Variational Interconnect Modeling and Analyses
Sponsor:	Semiconductor Research Corporation (SRC/GRC)
PI:	Peng Li
Co-PI:	Lawrence Pileggi (CMU)
Amount:	$370,000 (total) $183,542(Peng Li)
Period:	4/1/2005 – 7/31/2008

Project 1:	Parametric and Fault Simulation Framework for Analog Test Automation
Sponsor:	Center for Circuit and System Solutions (C2S2), SRC Focus Center Research Program (FCRP)
PI:	Peng Li
Amount:	$103,809
Period:	9/1/2004 – 8/31/2006

PUBLICATIONS

More than 200 published refereed journal and conference papers, and books/book chapters.

Supervised graduate students/post-doctoral fellows are delineated with an asterisk (*).

Selected Recent Publications (all publications listed later)

[NIPS'18] *Yingyezhe Jin, *Wenrui Zhang, and Peng Li, "Hybrid macro/micro level backpropagation for training deep spiking neural networks," In Proc. of Conference on Neural Information Processing Systems (NIPS), December 2018 (to appear) (acceptance rate 1011/4856 = 20.8%).

[ICCAD'18] *Hanbin Hu, Peng Li, and Jianhua Z. Huang, "Parallelizable Bayesian optimization for analog and mixed-signal rare failure detection with high coverage," in Proc. of IEEE/ACM Conf. on Computer-Aided Design, November 2018 (acceptance rate: 98/396 = 24.7%) (**Best Paper Award Nomination**).

[JETC'18] *Yu Liu, *Yingyezhe Jin, and Peng Li, "Online adaptation and energy minimization for hardware recurrent spiking neural networks," in ACM Journal on Emerging Technologies in Computing Systems, vo. 14, no. 1, pp. 11:1 – 11:21, Mar. 2018.

[TCAD'18] *Xin Zhan, Peng Li and E. Sánchez, "Taming the stability-constrained performance optimization challenge of distributed on-chip voltage regulation," in IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, 2018.

[DAC'18] *Hanbin Hu, *Qingran Zheng, *Ya Wang, and Peng Li, "HFMV: Hybridizing formal methods and machine Learning for verification of analog and mixed-signal circuits," in Proc. of IEEE/ACM Design Automation Conference (DAC), pp. 95:1--95:6, June 2018 (acceptance rate: 168/691 = 24.3%).

[DAC'18] Bon Woong Ku, *Yu Liu, *Yingyezhe Jin, Sandeep Samal, Peng Li, and Sung Kyu Lim, "Design and architectural co-optimization of monolithic 3D liquid state machine-based neuromorphic processor," in Proc. of IEEE/ACM Design Automation Conference (DAC), pp. 165:1--165:6, June 2018 (acceptance rate: 168/691 = 24.3%).

[IJCNN'17] *Yingyezhe Jin, and Peng Li, "Calcium-modulated supervised spike-timing-dependent plasticity for readout training and sparsification of the liquid state machine," In Proc. of International Joint Conference on Neural Networks, pp. 2007-2014, May 2017.

[DAC'16] *Xin Zhan, Peng Li, and Edgar Sanchez-Sinencio, "Distributed on-chip voltage regulation: theoretical stability foundation, over-design reduction and performance optimization," in Proc. of IEEE/ACM Design Automation Conference, pp. 54:1-54:6, June 2016 (**Best Paper Award**).

[ISCAS'16] *Qian Wang, *Youjie Li, and Peng Li, "Liquid state machine based pattern recognition on FPGA with firing-activity dependent power gating and approximate computing," in Proc. of IEEE Intl. Symposium of Circuits and Systems, pp. 361-364, May 2016. (**ISCAS Honorary Mention Best Paper Award from the Neural Systems and Applications Technical Committee of IEEE Circuits and Systems Society**).

Books

Peng Li, L. Miguel Silveira and Peter Feldmann (Eds.), *Simulation and Verification of Electronic and Biological Systems*, Springer, 2011.

Rasit O. Topaloglu and Peng Li (Eds.), *Recent Topics on Modeling of Semiconductor Processes, Devices and Circuits*, Bentham Publishing, 2011.

Full List of Refereed Journal Publications

[J66] *Wenrui Zhang and Peng Li, "Information-theoretic intrinsic plasticity for online unsupervised learning in spiking neural networks," Frontiers in Neuroscience, 2018 (under review).

[J65] [TCAD'18] *Xin Zhan, Peng Li and E. Sánchez, "Taming the stability-constrained performance optimization challenge of distributed on-chip voltage regulation," in IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, 2018.

[J64] [TVLSI'18] *Xin Zhan, Joseph Riad, Peng Li and E. Sánchez, "Design space exploration of distributed on-chip voltage regulation under stability constraint," in IEEE Trans. on Very Large Scale Integration Systems, 2018.

[J63] [QIP'18] Alexandre Y. Yamamoto, Kyle M. Sundqvist, Peng Li, and H. Rusty Harris, "Simulation of a multidimensional input quantum perceptron," in Quantum Information Processing, (2018) 17: 128.

[J62] [JETC'18] *Yu Liu, *Yingyezhe Jin, and Peng Li, "Online adaptation and energy minimization for hardware recurrent spiking neural networks," in ACM Journal on Emerging Technologies in Computing Systems, vo. 14, no. 1, pp. 11:1 – 11:21, Mar. 2018.

[J61] [IET'18] Changqing Xu, Yi Liu, Peng Li, and Yintang Yang, "Unified Multi-objective Mapping for Network-on-chip Using Genetic based Hyper-heuristic Algorithms," IET Computers & Digital Techniques, Jan. 2018.

[J60] [TODAS'17] *Ya Wang, *Di Gao, Dani Tannir, Ning Dong, G. Peter Fang, Wei Dong, and Peng Li, "Multi-harmonic small-signal modeling of low power PWM DC-DC converters," in ACM Trans. on Design Automation of Electronic Systems, vo. 22, issue 4, pp. 68:1-68:16, June 2017.

[J59] [NeuroComp'17] *Yingyezhe Jin and Peng Li, "Performance and robustness of bio-inspired digital liquid state machines: A case study of speech recognition," Neurocomputing, vo. 226, pp. 146-160, Feb. 2017.

[J58] [NeuroComp'17] *Qian Wang, *Youjie Li, *Botang Shao, *Siddhartha Dey, and Peng Li, "Energy efficient parallel neuromorphic architectures with approximate arithmetic on FPGA," Neurocomputing, vo. 221, pp. 146-158, Jan. 2017.

[J57] [TCAD'16] *Ya Wang and Peng Li, "Robust and efficient transistor-level envelope-following analysis of PWM/PFM/PSM DC-DC converters," in IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vo. 35, issue 11, pp. 1836-1847, Nov. 2016.

[J56] [D&T'16] *Parijat Mukherjee and Peng Li, "Using presilicon knowledge to excite nonlinear failure modes in large mixed-signal circuits," in IEEE Design & Test, vo. 33, issue 5, pp. 28-34, Oct. 2016.

[J55] [JETC'16] *Qian Wang, Yongtae Kim, and Peng Li, "Neuromorphic processors with memristive synapses: synaptic interface and architectural exploration," in ACM Journal on Emerging Technologies in Computing Systems, vo. 12, issue 14, pp. 35:1 – 35:22, Jul. 2016.

[J54] [TODAES'16] Dani A. Tannir, *Ya Wang, and Peng Li, "Accurate modeling of nonideal low power PWM DC-DC converters operating in CCM and DCM using enhanced circuit averaging techniques," in ACM Trans. on Design Automation of Electronic Systems. vo. 21, issue 4, pp. 61:1--61:15, May 2016.

[J53] [TNNLS'15] *Yong Zhang, Peng Li, *Yingyezhe Jin, and Yoonsuck Choe, "A digital liquid state machine with biologically inspired learning and its application to speech recognition," in IEEE Trans. on Neural Networks and Learning Systems, vol. 26, no. 11, pp. 2635-2649, Nov. 2015.

[J52][TVLSI'15] *Yongtae Kim, *Yong Zhang, and Peng Li, "Energy efficient approximate arithmetic

for error resilient neuromorphic computing," in IEEE Trans. on Very Large Scale Integration Systems, vol. 23, no. 11, pp. 2733-2737, Nov. 2015.

[J51] [TCAD'15] *Honghuang Lin and Peng Li, "Circuit performance classification with active learning guided sampling for support vector machines," in IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 34, no. 9, pp.1467-1480, Sep. 2015.

[J50] [TVLSI'15] *Qian Wang, Peng Li, and *Yongtae Kim, "A parallel digital VLSI architecture for integrated support vector machine training and classification," IEEE Trans. on Very Large Scale Integration Systems, vol. 23, no. 8, pp. 1471-1484, Aug. 2015.

[J49] [TODAES'15] *Tong Xu, Peng Li, and Savithri Sundareswaran, "Decoupling capacitance design strategies for power delivery networks with power gating," ACM Trans. on Design Automation of Electronic Systems, vol. 20, no. 3, pp. 38:1-38:30, Jun. 2015.

[J48] [TCAS1'15] *Botang Shao and Peng Li, "Array-based approximate arithmetic computing: A general model and applications to multiplier and squarer design," IEEE Trans. on Circuits and Systems I, 2014, vol. 62. no. 4, pp. 1081-1090, Apr. 2015.

[J47] [JETC'15] *Yongtae Kim, *Yong Zhang, and Peng Li, "A reconfigurable digital neuromorphic processor with memristive synaptic crossbar for cognitive computing," ACM Journal on Emerging Technologies in Computing Systems, vol. 11, no. 4, pp. 38:1-38:25, Apr. 2015.

[J46] [NN'15] Shiping Wen, Tingwen Huang, Zhigang Zhang, Yiran Chen, and Peng Li, "Circuit design and exponential stabilization of memristive neural networks," Neural Networks, vol. 63, pp. 48-56, 2015.

[J45] [TODAS'14]Yenpo Huang, Garng M. Huang, and Peng Li, "Understanding SRAM stability via bifurcation analysis: analytical models and scaling trends," ACM Trans. on Design Automation of Electronic Systems, vol. 19, no. 4, pp. 41:1-41:25, Aug. 2014.

[J44] [TCAD'13] *Suming Lai, *Boyuan Yan, and Peng Li, "Localized stability checking and design of IC power delivery with distributed voltage regulators," IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, pp. 1321-1333, September 2013.

[J43][TVLSI'13] *Zhuo Feng and Peng Li, "Fast thermal analysis on GPU for 3D-ICs with integrated microchannel cooling," IEEE Trans. on Very Large Scale Integration Systems, volume 21, issue 8, pp. 1526-1539, August 2013.

[J42] [TCAD'13] *Leyi Yin, *Yue Deng, and Peng Li, "Simulation-assisted formal verification of nonlinear mixed-signal circuits with Bayesian inference guidance," IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, pp. 977-990, July 2013.

[J41] [AICSP'13] *Yongtae Kim and Peng Li, "A 0.003-mm2, 0.35-V, 82-pJ/conversion ultra-low power CMOS all digital temperature sensor for on-die thermal management," Analog Integrated Circuits and Signal Processing, volume 75, issue 1, pp 147-156, April 2013.

[J40] [TODAES'13] *Zhiyu Zeng, *Suming Lai, and Peng Li, "IC power delivery: voltage regulation and conversion, system-level co-optimization and technology implications," in ACM Trans. on Design Automation of Electronic Systems, volume 18, issue 2, pp. 29:1 – 29:21, March 2013.

[J39] [NeuroImage'13] *Boyuan Yan and Peng Li, "The emergence of abnormal hypersynchronization

in the anatomical structural network of human brain," NeuroImage, volume 65, pp. 34-51, January 2013 (impact factor: 6.608).

[J38] [IET-CDS'13] *Yongtae Kim and Peng Li, "'A 0.38-V Near/Sub-VT Digitally Controlled Low-Dropout Regulator with Enhanced Power Supply Noise Rejection in 90-nm CMOS Process," IET Circuits, Devices and Systems, volume 7, issue 1, pp. 31-41, January 2013.

[J37] [NeuroComp'12] *Yong Zhang, *Boyuan Yan, *Mingchao Wang, *Jingzhen Hu, *Haokai Lu, and Peng Li, "Linking brain behavior to underlying cellular mechanisms via large-scale brain modeling and simulation," Neurocomputing, vo. 97, pp. 317-331, Nov. 2012.

[J36] [TCAD'12] *Parijat Mukherjee, G. Peter Fang, Rod Burt, and Peng Li, "Efficient identification of unstable loops in large linear analog integrated circuits," in IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 31, issue 9, pp. 1332-1345, September 2012.

[J35] [AICSP'12] *Suming Lai and Peng Li, "A fully on-chip area-efficient CMOS low-dropout regulator with fast load regulation," Analog Integrated Circuits and Signal Processing, vol. 72, no. 2 (2012), 433-450, DOI: 10.1007/s10470-012-9841-8.

[J34] [JCP'11] *Haokai Lu and Peng Li, "Stochastic projective methods for simulating stiff chemical reacting systems," Computer Physics Communications, vol. 183, issue 7, pp. 1427–1442, July 2012.

[J33] [TCBB'11] *Yong Zhang, Peng Li, and Garng M. Huang, "Quantifying dynamic stability of genetic memory circuits," IEEE/ACM Transactions on Computational Biology and Bioinformatics, vol. 9, issue 3, pp. 871-884, May 2012.

[J32] [FTEDA'12] Peng Li, "Parallel Circuit Simulation: A Historical Perspective and Recent Developments," Foundations and Trends in Electronic Design Automation: vol. 5: no. 4, pp 211-318, Apr. 2012 (**invited**).

[J31] [TODAES'11] *Wei Dong and Peng Li, "Parallel circuit simulation with adaptively controlled projective integration," in ACM Trans. on Design Automation of Electronic Systems, vol. 16, no.4, October 2011.

[J30] [PLoS One'11] *Boyuan Yan and Peng Li, "An integrative view of epileptic genesis and its implication on optimal therapeutic treatments," PLoS One 6(7): e22440. doi:10.1371/journal.pone.0022440.

[J29] [TVLSI'11] Zhuo Feng, *Zhiyu Zeng, and Peng Li, "Parallel on-chip power distribution network analysis on multi-core-multi-GPU platforms," in IEEE Trans. on Very Large Scale Integration Systems, vol. 19, no. 10, pp. 1823-1836, October 2011.

[J28] [TODAES'11] *Zhiyu Zeng, Zhuo Feng, Peng Li and Vivek Sarin, "Locality-driven parallel static analysis for power delivery networks," in ACM Trans. on Design Automation of Electronic Systems, vol. 16, no. 3, pp. 28:1--28:17, June 2011.

[J27] [TCAS'11] Yenpo Ho, Garng M. Huang, and Peng Li, "Dynamical properties and design analysis for nonvolatile memristor memories," in IEEE Trans. on Circuits and Systems I: Fundamental Theory and Applications, vol. 58, no. 4, pp. 724-736, April 2011.

[J26] [TCAD'11] *Guo Yu and Peng Li, "Hierarchical analog/mixed-signal circuit optimization under

process variations and tuning," in IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 30, no. 2, pp. 313-317, February, 2011.

[J25] [JCNS'11] *Boyuan Yan and Peng Li, "Reduced order modeling of passive and quasi-active dendrites for nervous system simulation," J Comput Neurosci (2011) 31:247–271.

[J24] [TCAD'11] *Xaioji Ye, *Wei Dong, Peng Li, and Sani Nassif, "Hierarchical multialgorithm parallel circuit simulation," in IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 30, issue 1, pp. 45-58, January 2011.

[J23] [TCAD'10] *Xaioji Ye, Peng Li, Min Zhao, Rajendran Panda, and Jiang Hu, "Scalable analysis of mesh-based clock distribution networks using application-specific reduced order modeling," in IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems , vol. 29, no. 9, pp. 1342-1353, September 2010 (**TCAD best paper award nomination**).

[J22] [TVLSI'10] Rupak Samanta, Jiang Hu, and Peng Li, "Discrete buffer and wire sizing for link-based non-tree clock networks," in IEEE Trans. on Very Large Scale Integration Systems, vol. 18, no. 7, pp. 1025 – 1035, July 2010.

[J21] [JLPE'10] *Akshit Dayal, Peng Li, and Garng M. Huang, "Robust SRAM design via joint sizing and voltage optimization under dynamic stability constraints," in Journal of Low Power Electronics, vol. 6, no. 1, Apr. 2010.

[J20] [JLPE'10] *Guo Yu and Peng Li, "Exploring circuit adaptation for yield optimization of low-power all-digital PLLs," Journal of Low Power Electronics, vol. 6, no. 1, Apr. 2010.

[J19] [TCAS'10] *Xiaoji Ye, Peng Li, and Frank Liu, "Exact time-domain second-order adjoint sensitivity computation for linear circuit analysis and optimization," in IEEE Trans. on Circuits and Systems I: Fundamental Theory and Applications, vol. 57, no. 1, pp. 236-248, January 2010.

[J18][TVLSI'09] Ganesh Venkataraman, *Zhuo Feng, Jiang Hu, and Peng Li, "Combinatorial algorithms for fast clock mesh optimization," in IEEE Trans. on Very Large Scale Integration Systems, vol. 18, no. 1, pp. 131-141, Jan. 2010.

[J17] [IET'09] *Zhuo Feng, Peng Li, and Zhuoxiang Ren, "SICE: design-dependent statistical interconnect corner extraction under inter/intra-die variations," IET Circuits, Devices & Systems, vol. 3, issue. 5, pp. 248-258, 2009.

[J16] [TCAD09]*Zhiyu Zeng and Peng Li, "Locality-driven parallel power grid optimization," in IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 28, no. 8, pp. 1190-1200, August 2009.

[J15] [TCAD'09] *Wei Dong and Peng Li, "A parallel harmonic balance approach to steady-state and envelope-following simulation of driven and autonomous circuits," in IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 28, no. 4, pp. 490-501, April 2009.

[J14] [TCAD'09] *Zhuo Feng, Peng Li, and Yaping Zhan, "An on-the-fly parameter dimension reduction approach to fast second-order statistical static timing analysis," in IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 28, no. 1, pp. 141-153, January 2009.

[J13] [TVLSI'09] *Zhuo Feng and Peng Li, "Performance-oriented parameter dimension reduction of VLSI circuits," in IEEE Trans. on Very Large Scale Integration Systems, vol. 17, no. 1, pp. 137-150, January 2009.

[J12] [TCAD'08] Yang Yi, Peng Li, Vivek Sarin, and Weiping Shi, "A preconditioned hierarchical algorithm for impedance extraction of three-dimensional structures with multiple dielectrics," in IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 27, no. 11, pp. 1918 – 1927, November 2008.

[J11] [TCAD'08] *Guo Yu, *Wei Dong, *Zhuo Feng, and Peng Li, "Statistical static timing analysis considering process variation model uncertainty," in IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 27, no. 10, pp. 1880-1890, October 2008.

[J10] [TCAD'07] *Wei Dong and Peng Li, "Hierarchical harmonic balance methods for frequency-domain analog circuits analysis," in IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 26, no. 12, pp. 2089-2101, December. 2007.

[J9] [TVLSI'07] Peng Li, *Zhuo Feng, and Emrah Acar, "Characterizing multi-stage nonlinear drivers and variability for accurate timing and noise analysis," in IEEE Trans. on Very Large Scale Integration Systems, vol. 15, no. 11, pp. 1205-1214, November 2007.

[J8] [TVLSI'07] Shiyan Hu, Qiuyang Li, Jiang Hu, and Peng Li, "Utilizing redundancy for timing critical interconnect," in IEEE Trans. on Very Large Scale Integration Systems, vol. 15, no. 10, pp. 1067-1080, October 2007.

[J7] [TVLSI'07] *Xiaoji Ye, Frank Liu, and Peng Li, "Fast variational interconnect delay and slew computation using quadratic models," in IEEE Trans. on Very Large Scale Integration Systems, vol. 15, no. 8, pp. 913-926, August 2007.

[J6] [TCAS'07] *Guo Yu and Peng Li, "Efficient lookup table based modeling for robust design of Sigma-Delta ADCs," in IEEE Trans. on Circuits and Systems I: Fundamental Theory and Applications, vol. 54, no. 7, pp. 1513-1528, July 2007.

[J5] [TCAD'06] Peng Li, "Statistical sampling-based parametric analysis of power grids," in IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 25, no. 12, pp. 2852-2867, December 2006.

[J4] [TCAD'06] Peng Li, Lawrence Pileggi, Mehdi Asheghi, and Rajit Chandra, "IC thermal simulation and modeling via efficient multigrid-based techniques," in IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 25, no. 9, pp. 1763-1776, September, 2006.

[J3] [JLOPE'06] Yangdong Deng and Peng Li, "Temperature-aware floorplanning of 3-D ICs considering thermally dependent leakage power," Journal of Low Power Electronics, vol. 2, no.2, August 2006.

[J2] [TCAD'05] Peng Li and Lawrence Pileggi, "Compact reduced-order modeling of weakly nonlinear analog and RF circuits," in IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol. 23, no. 2, pp. 184-203, Feb, 2005 (**The most downloaded IEEE TCAD publication in 2005**).

[J1] [TCAD'03] Peng Li and Lawrence Pileggi, "Efficient per-nonlinearity distortion analysis for analog and RF circuits," in IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, vol.

22, no. 10, pp. 1297-1309, October 2003.

Full List of Refereed Conference and Workshop Papers

[C144] Myung Seok Shim, and Peng Li, "Optimized gated deep learning architectures for sensor fusion," International Conference on Learning Representations (ICLR), 2019 (submitted).

[C143] T.J. Chang, Yukun He, and Peng Li, "Efficient two-step adversarial defense for deep neural networks," International Conference on Learning Representations (ICLR), 2019 (submitted).

[C142][NIPS'18] *Yingyezhe Jin, *Wenrui Zhang, and Peng Li, "Hybrid macro/micro level backpropagation for training deep spiking neural networks," In Proc. of Conference on Neural Information Processing Systems (NIPS), December 2018 (to appear) (acceptance rate 1011/4856 = 20.8%).

[C141][ICCAD'18] *Hanbin Hu, Peng Li, and Jianhua Z. Huang, "Parallelizable Bayesian optimization for analog and mixed-signal rare failure detection with high coverage," in Proc. of IEEE/ACM Conf. on Computer-Aided Design, November 2018 (acceptance rate: 98/396 = 24.7%).

[C140] [ICCAD'18] Bon Woong Ku, *Yu Liu, *Yingyezhe Jin, Peng Li, and Sung Kyu Lim, "Area-efficient and Low-power Face-to-Face-bonded 3D liquid state machine Design," in Proc. of IEEE/ACM Conf. on Computer-Aided Design, November 2018 (acceptance rate: 98/396 = 24.7%).

[C139][Techcon'18] *Yu, Liu, and Peng Li, "Performance Enhancement for FPGA recurrent spiking neural accelerators with supervised and unsupervised spike-timing-dependent plasticity," 4 pages, Semiconductor Research Corporation TECHCON Conference, 4 pages, September 2018.

[C138][Techcon'18] *Hanbin Hu, and Peng Li, "A hybrid verification framework for analog and mixed-signal circuits," 4 pages, Semiconductor Research Corporation TECHCON Conference, 4 pages, September 2018.

[C137][DAC'18] Bon Woong Ku, *Yu Liu, *Yingyezhe Jin, Sandeep Samal, Peng Li, and Sung Kyu Lim, "Design and architectural co-optimization of monolithic 3D liquid state machine-based neuromorphic processor," in Proc. of IEEE/ACM Design Automation Conference (DAC), pp. 165:1--165:6, June 2018 (acceptance rate: 168/691 = 24.3%).

[C136][DAC'18] *Hanbin Hu, *Qingran Zheng, *Ya Wang, and Peng Li, "HFMV: Hybridizing formal methods and machine Learning for verification of analog and mixed-signal circuits," in Proc. of IEEE/ACM Design Automation Conference (DAC), pp. 95:1--95:6, June 2018 (acceptance rate: 168/691 = 24.3%).

[C135] [Techon'17] *Yu Liu, *Yingyezhe Jin, and Peng Li, "Energy minimization for self-organizing recurrent spiking neural processors," Semiconductor Research Corporation TECHCON Conference, 4 pages, September 2017.

[C134] [ISLPED'17] *Yu Liu, *Yingyezhe Jin, and Peng Li, "Exploring sparsity of firing activities and clock gating for energy-efficient recurrent spiking neural processors," in Proc. of IEEE/ACM Intl. Symp. on Low Power Electronics and Design (ISLPED), pp.1-6, July 2017.

[C133][DAC'17] *Ya Wang, Peng Li, and Jian Gong, "Convergence-boosted graph partitioning using maximum spanning trees for iterative solution of large linear circuits," in Proc. of IEEE/ACM Design

Automation Conference (DAC), pp. 69:1--69:6, June 2017.

[C132][IJCNN'17] *Yingyezhe Jin, and Peng Li, "Calcium-modulated supervised spike-timing-dependent plasticity for readout training and sparsification of the liquid state machine," In Proc. of International Joint Conference on Neural Networks, pp. 2007-2014, May 2017.

[C131][IJCNN'17] *Myung Seok Shim, and Peng Li, "Biologically inspired reinforcement learning for mobile robot collision avoidance," In Proc. of International Joint Conference on Neural Networks, pp. 3098-3105, May 2017.

[C130][IJCNN'17] *Amarnath Mahadevuni, and Peng Li, "Navigating mobile robots to target in near shortest time using reinforcement learning with spiking neural networks," In Proc. of International Joint Conference on Neural Networks, pp. 2243-2250, May 2017.

[C129][ICICDT'17] Honghuang Lin, Asad M. Khan, and Peng Li, "Statistical circuit performance dependency analysis via sparse relevance kernel machine," in Proc. of IEEE International Conference on IC Design and Technology (ICICDT), pp. 1-4, May 2017 (invited).

[C128] [DATE'17] *Ang Li, Peng Li, Tingwen Huang, and Edgar Sanchez-Sinencio, "Noise-sensitive feedback loop identification in linear time-varying analog circuits," in Proc. of IEEE/ACM Design Automation and Test In Europe Conference & Exhibition (DATE), pp. 1285-1288, March 2017.

[C127][ICPR'16] *Qian Wang, and Peng Li, "D-LSM: Deep liquid state machine with unsupervised recurrent reservoir tuning," In Proc. of The International Conference on Pattern Recognition, pp. 1158-1165, December 2016.

[C126][IJCNN'16] *Yingyezhe Jin, and Peng Li, "AP-STDP: A novel self-organizing mechanism for efficient reservoir computing," In Proc. of The International Joint Conference on Neural Networks, pp. 1158-1165, July 2016.

[C125][NanoARCH'16] *Yingyezhe Jin, *Yu Liu, and Peng Li, "SSO-LSM: A sparse and self-organizing architecture for liquid state machine based neural processors," In Proc. of IEEE/ACM International Symposium on Nanoscale Architectures, pp. 55-60, July 2016.

[C124][DAC'16] *Xin Zhan, Peng Li, and Edgar Sanchez-Sinencio, "Distributed on-chip voltage regulation: theoretical stability foundation, over-design reduction and performance optimization," in Proc. of IEEE/ACM Design Automation Conference, pp. 54:1-54:6, June 2016 (**Best Paper Award**).

[C123][DAC'16] *Honghuang Lin and Peng Li, "Relevance vector and feature machine for statistical analog circuit characterization and built-in self-test optimization," in Proc. of IEEE/ACM Design Automation Conference, pp. 11:1-11:6, June 2016.

[C122][ISCAS'16] *Qian Wang, *Youjie Li, and Peng Li, "Liquid state machine based pattern recognition on FPGA with firing-activity dependent power gating and approximate computing," in Proc. of IEEE Intl. Symposium of Circuits and Systems, pp. 361-364, May 2016. (**ISCAS Honorary Mention Best Paper Award from the Neural Systems and Applications Technical Committee of IEEE Circuits and Systems Society**).

[C121] [DATE'16] *Ya Wang, *Di Gao, Dani A. Tannir, and Peng Li, "Multi-harmonic nonlinear modeling of low-power PWM DC-DC converters operating in CCM and DCM," in Proc. of Design Automation and Test In Europe Conference & Exhibition (DATE), pp. 409 – 414, March 2016, (long

presentation, acceptance rate 24%).

[C120] [FAC'15] *Parijat Mukherjee and Peng Li, "Functional testing of large mixed-signal circuits with non-linear dynamics using pre-silicon knowledge," Frontiers in Analog CAD (FAC) Workshop, 2 pages, November 2015.

[C119][BioCAS'15] *Qian Wang, *Yingyezhe Jin, and Peng Li, "General-purpose LSM learning processor architecture and theoretically guided design space exploration," in Proc. of IEEE Biomedical Circuits and Systems Conference, pp. 1-4, Oct. 2015 (lecture presentation; acceptance rate 13.0%, 45/345).

[C118] [TECHCON'15] *Honghuang Lin and Peng Li, "Classifying circuit performance using active-learning guided support vector machines," Semiconductor Research Corporation TECHCON Conference, 4 pages, September 2015.

[C117][NFM'15] Andrew Fisher, Chris Myers, and Peng Li, "Reachability analysis using extremal rates," in Proc. of NASA Formal Methods Symposium, April 2015 (acceptance rate: 30.6%).

[C116][ICCAD'14] *Ya Wang, Peng Li, and *Suming Lai, "A Unifying and robust method for efficient envelope-following simulation of PWM/PFM DC-DC converters," in Proc. of IEEE/ACM Conf. on Computer-Aided Design, pp. 618-625, November 2014 (acceptance rate: 25.3%, 77/304).

[C115][IEEENano'14] *Qian Wang, *Yongtae Kim, and Peng Li, "Architectural design exploration for neuromorphic processors with memristive synapses," in Proc. of IEEE Intl. Conference on Technology, pp. 962-966, August 2014.

[C114][ISLPED'14] *Botang Shao and Peng Li, "A model for array-based approximate arithmetic computing with application to multiplier and squarer design," in Proc. of IEEE/ACM Intl. Symp. on Low Power Electronics and Design (oral presentation), pp. 9-14, August 2014 (acceptance rates: 23%(oral presentation), 34% (overall)).

[C113][MWSCAS'14] *Ahmad Bashaireh and Peng Li, "Design robustness analysis of digital spiking neural circuits," in Proc. of IEEE Int'l Midwest Symposium on Circuits & Systems, pp. 737-740, August 2014.

[C112][DAC'14] *Parijat Mukherjee, Chirayu Amin, and Peng Li, "Approximate property checking of mixed-signal circuits," in Proc. of IEEE/ACM Design Automation Conference, pp. 1-6, June 2014 (acceptance rate: 22.1/%, 174/787) and also in Proc. of ACM Int. Workshop on Timing Issues in the Specification and Synthesis of Digital Systems, March 2014.

[C111][DAC'14] *Honghuang Lin and Peng Li, "Parallel hierarchical reachability analysis for analog verification," in Proc. of IEEE/ACM Design Automation Conference, pp. 1-6, June 2014 (acceptance rate: 22.1/%, 174/787).

[C110][TAU'14] *Parijat Mukherjee and Peng Li, "Leveraging pre-silicon data to diagnose out-of-specification failures in mixed-signal circuits," in Proc. of IEEE/ACM Design Automation Conference, pp. 1-6, June 2014 (acceptance rate: 22.1/%, 174/787).

[C109][ICCAD'13] *Yongtae Kim, *Yong Zhang, and Peng Li, "An energy efficient approximate adder with carry skip for error resilient neuromorphic VLSI systems," in Proc. of IEEE/ACM Conf. on Computer-Aided Design, pp. 130-137, November 2013 (acceptance rate: 26.0%, 92/354).

[C108][BioMedCom'13] *Shaoda Yu, Peng Li, *Honghuang Lin, Ehsan Rohani, Gwan Choi, *Botang Shao, and *Qian Wang, "Support vector machine based detection of drowsiness using minimum EEG features," ASE/IEEE Intl. Conf. on Biomedical Computing, pp. 827-835, September 2013.

[C107] [TECHCON0'13] *Yongtae Kim, *Yong Zhang, and Peng Li, "A brain-inspired digital neuromorphic VLSI architecture with memristive crossbar for cognitive computing," Semiconductor Research Corporation TECHCON Conference, 4 pages, September 2013.

[C106] [TECHCON0'13] *Parijat Mukherjee, Chirayu Amin, and Peng Li, "A formal approach to DC operating point analysis for large mixed signal circuits: challenges and opportunities," Semiconductor Research Corporation TECHCON Conference, 4 pages, September 2013.

[C105] [TECHCON0'13] *Suming Lai, *Boyuan Yan, and Peng Li, "Stability-ensured design methodology for distributed on-chip linear voltage regulators in modern IC power delivery networks," Semiconductor Research Corporation TECHCON Conference, 4 pages, September 2013.

[C104][DAC'13] *Honghuang Lin, Peng Li, and Chris J. Myers, "Verification of digitally-intensive analog circuits via kernel ridge regression and hybrid reachability analysis," in Proc. of IEEE/ACM Design Automation Conf., pp. 1-6, May 2013 (acceptance rate: 21.7%, 162/747).

[C103] [TAU'13] *Parijat Mukherjee, Chirayu Amin, and Peng Li, "A formal approach to DC operating point analysis for large mixed signal circuits: challenges and opportunities," in Proc. of ACM Int. Workshop on Timing Issues in the Specification and Synthesis of Digital Systems, March 2013.

[C102] [FAC'13] *Honghuang Lin and Peng Li, "Reachability analysis for AMS verification using hybrid support function and SMT-based method," Frontiers in Analog CAD (FAC) Workshop, 2 pages, February 2013.

[C101] [ISQED'13] *Suming Lai and Peng Li, "A power-efficient on-chip linear regulator assisted by switched capacitors for fast transient regulation," in Proc. of IEEE Symp. on Quality Electronic Design, pp. 682-688, March 2013.

[C100][ICCAD'12] *Suming Lai, *Boyuan Yan, and Peng Li, "Stability assurance and design optimization of large power delivery networks with multiple on-chip voltage regulators," IEEE/ACM Intl. Conf. on Computer-Aided Design, pp. 247-254, November 2012 (acceptance rate: 24.3%, 82/338)
(**IEEE/ACM William J. McCalla ICCAD Best Paper Award, one out of 338 submissions**).

[C99][ICCAD'12] Peng Li, "Design analysis of IC power delivery," IEEE/ACM Conf. on Computer-Aided Design (invited paper), pp. 664-666, November 2012.

[C98][ICCAD'12] *Leyi Yin, *Yue Deng, and Peng Li, "Verifying dynamic properties of nonlinear mixed-signal circuits via efficient SMT-based techniques," IEEE/ACM Conf. on Computer-Aided Design, pp. 436-442, November 2012 (acceptance rate: 24.3%, 82/338).

[C97][ICCAD'12] *Honghuang Lin and Peng Li, "Classifying circuit Performance using active-learning guided support vector machines," IEEE/ACM Conf. on Computer-Aided Design, pp. 187-194, November 2012 (acceptance rate: 24.3%, 82/338).

[C96] [VLSI-SoC'12] Bin Wu and Peng Li, "Load-aware stochastic feedback control for DVFS with tight performance guarantee," IEEE/ IFIP Int. Conf. on VLSI and System-on-Chip, pp. 231-236,

October 2012.

[C95] [TECHCON0'12] *Tong Xu and Peng Li, "Design tradeoffs and strategies of power gating with DVFS," Semiconductor Research Corporation TECHCON Conference, 4 pages, September 2012.

[C94] [TECHCON0'12] *Yongtae Kim and Peng Li, "An on-chip variation tolerant digital LDO regulator for extremely low voltage applications," Semiconductor Research Corporation TECHCON Conference, 4 pages, September 2012.

[C93] [SOCC'12] *Yongtae Kim, *Yong Zhang, and Peng Li, "A digital neuromorphic VLSI architecture with memristor crossbar synaptic array of machine learning", IEEE Int. System-on-Chip Conf., pp. 328-333, September 2012.

[C92] [ICDCT'12] *Suming Lai, Peng Li, and Zhiyu Zeng, "Design and analysis of IC power delivery with on-chip voltage regulation," International Conference on IC Design and Technology, pp. 1-4, May 2012 (invited).

[C91] [ISQED'12] *Yongtae Kim and Peng Li, "An ultra-Low voltage digitally controlled low-dropout regulator with digital background calibration," in Proc. of IEEE Symp. on Quality Electronic Design, pp. 151-158, March 2012.

[C90] [ISQED'12] *Tong Xu and Peng Li, "Design and optimization of power gating for DVFS applications," in Proc. of IEEE Symp. on Quality Electronic Design, pp. 391-397, March 2012.

[C89] [ICCAD'11] *Zhiyu Zeng, *Tong Xu, Zhuo Feng, and Peng Li, "Fast static analysis of power grids: algorithms and implementations," in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 488-493, November 2011 (invited).

[C88] [TECHCON0'11] *Zhiyu Zeng, *Suming Lai, and Peng Li, "IC power delivery: voltage regulation, conversion and system-level co-optimization," Semiconductor Research Corporation TECHCON Conference, 4 pages, September 2011.

[C87] [IJCNN'11] *Mingchao Wang, *Boyuan Yan, *Jingzhen Hu and Peng Li, "Simulation of large neuronal networks with biophysically accurate models on graphics processors," IEEE International Joint Conference on Neural Networks, pp. 3184-3193, July 2011.

[C86] [DAC'11] *Parijat Mukherjee, Peter Fang, Rod Burt, and Peng Li, "Automatic stability checking for large linear analog integrated circuits," IEEE/ACM Design Automation Conference, pp. 304-309, June 2011 (acceptance rate 22.6%) (**Best paper award, 1 out of 690 submissions, <1%**).

[C85] [DAC'11] *Tong Xu, Peng Li, and *Boyuan Yan, "Decoupling for power gating: sources of power noise and design strategies," IEEE/ACM Design Automation Conference, pp. 1002-1007, June 2011 (acceptance rate 22.6%).

[C84] [DAC'11] *Leyi Yin, *Yongtae Kim, and Peng Li "High effective-resolution built-in jitter characterization with quantization noise shaping," IEEE/ACM Design Automation Conference, pp. 765-770, June 2011 (acceptance rate 22.6%).

[C83] [TAU'11] *Tong Xu, Peng Li, and *Boyuan Yan, "Decoupling strategies for reducing power gating induced supply noise," in Proc. of ACM Int. Workshop on Timing Issues in the Specification and Synthesis of Digital Systems, March 2011.

[C82] [ISQED'11] *Leyi Yin and Peng Li, "RF BIST for ADPLL-based polar transmitters with wide-band DCO gain calibration," in Proc. of IEEE Int. Symp. on Quality Electronic Design, pp. 303-340, March 2011.

[C81] [ISQED'11] *Zhiyu Zeng, Zhuo Feng, and Peng Li, "Efficient checking of power delivery integrity for power gating," in Proc. of IEEE Int. Symp. on Quality Electronic Design, pp. 663-670, March 2011.

[C80] [ICCAD'10] *Xiaoji Ye and Peng Li, "On-the-fly runtime adaptation for efficient execution of parallel multi-algorithm circuit simulation," in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 298-304, November 2010 (acceptance rate 30%).

[C79] [ICCAD'10] *Amandeep Singh and Peng Li, "On behavioral model equivalence checking for large analog/mixed signal systems," in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 55-61, November 2010 (acceptance rate 30%).

[C78] [ICCAD'10] Zhuo Feng and Peng Li, "Fast thermal analysis on GPU for 3D-ICs with integrated microchannel cooling," in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 551-555, November 2010 (acceptance rate 30%).

[C77] [TECHCON0'10] *Zhiyu Zeng, Zhuo Feng, and Peng Li, "Tradeoff analysis and optimization of power delivery networks with on-chip voltage regulation," Semiconductor Research Corporation TECHCON Conference, 4 pages, September 2010.

[C76] [TECHCON0'10] *Leyi Yin and Peng Li, "In-situ jitter test and diagnosis of digital PLLs using digital reconfiguration," Semiconductor Research Corporation TECHCON Conference, 4 pages, September 2010.

[C75] [ICCCAS'10] Yenpo Ho, Garng M. Huang, and Peng Li, "Memristor system properties and its design applications to circuits such as nonvolatile memristor memories," in Proc. of IEEE Int. Conf. on Communications, Circuits and Systems, pp. 805-819, July 2010 (invited).

[C74] [DAC'10] *Leyi Yin and Peng Li, "Exploiting reconfigurability for low-cost in-situ test and monitoring of digital PLLs," in Proc. of ACM/IEEE Design Automation Conf., pp. 929-934, June 2010 (acceptance rate 24.4%).

[C73] [DAC'10] *Zhiyu. Zeng, *Xiaoji Ye, Zhuo Feng, and Peng Li, "Tradeoff analysis and optimization of power delivery networks with on-chip voltage regulation," in Proc. of ACM/IEEE Design Automation Conf., pp. 831-836, June 2010 (acceptance rate 24.4%).

[C72] [DAC'10] *Xiaoji Ye and Peng Li, "Parallel program performance modeling for runtime optimization of multi-algorithm circuit simulation," in Proc. of ACM/IEEE Design Automation Conf., pp. 561-566, June 2010 (acceptance rate 24.4%).

[C71] [DAC'10] *Yong Zhang, Peng Li, and Garng M. Huang, "Separatrices in high-dimensional state space: system-theoretical tangent computation and application to SRAM dynamic stability analysis," pp. 567-572, in Proc. of ACM/IEEE Design Automation Conf., June 2010 (acceptance rate 24.4%).

[C70] [TAU'10] *Xiaoji Ye and Peng Li, "Performance modeling of a hierarchical multi-algorithm parallel circuit simulator," in Proc. of ACM Int. Workshop on Timing Issues in the Specification and Synthesis of Digital Systems, March 2010 (acceptance rate 50%).

[C69] [ISPD'10] Venkata Rajesh Mekala, Yifang Liu, *Xiaoji Ye, Jiang Hu, and Peng Li, "Accurate

clock mesh sizing via sequential quadratic programming," in Proc. of ACM Int. Symp. on Physical Design, pp. 135-142, March 2010.

[C68] [ICCAD'09] *Yong Zhang and Peng Li, "Gene-regulatory memories: electrical-equivalent modeling, simulation and parameter identification," in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 491-496, November 2009 (acceptance rate 26.3%).

[C67] [ICCAD'09] *Wei Dong and Peng Li, "Final-value ODEs: stable numerical integration and its application to parallel circuit analysis," in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 403-409, November 2009 (acceptance rate 26.3%).

[C66] [ICCAD'09] *Xiaoji Ye, *Srinath S. Narasimhan, and Peng Li, "Leveraging efficient parallel pattern search for clock mesh optimization," in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 529-534, November 2009 (acceptance rate 26.3%).

[C65] [ICCAD'09] Yenpo Ho, Garng M. Huang, and Peng Li, "Nonvolatile memristor memory: device characteristics and design implications," in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 485-490, November 2009 (acceptance rate 26.3%).

[C64] [TECHCON'09] *Xioaji Ye, Wei Dong, and Peng Li, "A hierarchical multi-Algorithm parallel circuit simulation framework," Semiconductor Research Corporation TECHCON Conference, 4 pages, September 2009 (**Best in Session Award**).

[C63] [TECHCON'09] *Guo Yu and Peng Li, "Hierarchical synthesis of large mixed-signal circuits with consideration of process variations," Semiconductor Research Corporation TECHCON Conference, 4 pages, November 2009.

[C62] [DAC'09] *Wei Dong and Peng Li, "Parallelizable stable explicit numerical integration for efficient circuit simulation," in Proc. of IEEE/ACM Design Automation Conf., pp. 382-385, July 2009 (acceptance rate 21.7%).

[C61] [ISQED'09] *Zhiyu Zeng, Peng Li, and *Zhuo Feng, "Parallel partitioning based on-chip power distribution network analysis using locality acceleration," in Proc. of IEEE Int. Symp. on Quality Electronic Design, pp. 776-781, March 2009 (acceptance rate 29.0%).

[C60] [ISQED'09] *Xiaoji Ye and Peng Li, "An application-specific adjoint sensitivity analysis framework for clock mesh sensitivity computation," in Proc. of IEEE Int. Symp. on Quality Electronic Design, pp. 634-640, March 2009 (acceptance rate 29.0%).

[C59] [FPGA'09] Kanupriya Gulati, Sunil P. Khatri, and Peng Li, "Closed-loop modeling of power and temperature profiles of FPGAs," ACM/SIGDA Int. Symp. on Field-Programmable Gate Arrays, 9 pages, February 2009.

[C58] [ICCAD'08] *Zhuo Feng and Peng Li, "Multigrid on GPU: tackling power grid analysis on parallel SIMT platforms," in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 647-654, November 2008, (acceptance rate 26.6%) (**Best paper award nomination, 14 out of 458 submissions, 3%).**

[C57] [ICCAD'08] *Wei Dong, Peng Li, and Garng M. Huang, "SRAM dynamic stability: theory, variability and analysis," in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 378-385, November 2008 (acceptance rate 26.6%) (**Best paper award nomination, 14 out of 458**

submissions, 3%).

[C56] [ICCAD'08] *Guo Yu and Peng Li, "Yield-aware hierarchical optimization of large analog integrated circuits," in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 79-84, November 2008 (acceptance rate 26.6%).

[C55] [ICCAD'08] *Xiaoji Ye, *Wei Dong, Peng Li, and Sani R. Nassif, "MAPS: multi-algorithm parallel circuit simulation," in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 73-78, November 2008 (acceptance rate 26.6%).

[C54] [TECHCON'08] *Zhuo Feng, Peng Li, and Zhuoxiang Ren, "Design-dependent statistical interconnect corner extraction under inter/intra-die variations," Semiconductor Research Corporation TECHCON Conference, 4 pages, November 2008.

[C53] [DAC'08] *Wei Dong, Peng Li, and *Xiaoji Ye, "WavePipe: parallel transient simulation of analog and digital circuits on multi-core shared-memory machines," in Proc. of IEEE/ACM Design Automation Conf., pp. 238-243, June 2008 (acceptance rate 23.0%).
(**Best paper award, two out of 639 submissions, 0.3%**).

[C52] [ISCAS'08] Rajesh Garg, Peng Li, and Sunil P. Khatri "Modeling dynamic stability of SRAMs in the presence of single event upsets (SEUs)", in Proc. of IEEE Int. Symp. on Circuits and Systems, pp. 1788-1791, May 2008.

[C51] [ISPD'08] Rupak Samanta, Jiang Hu, and Peng Li, "Discrete buffer and wire sizing for link-based non-tree clock networks," ACM Int. Symp. on Physical Design, pp. 175-181, April 2008.

[C50] [ICCDCS'08] Ivick Guerra-Gomez, Esteban Tlelo-Cuautle, Peng Li, and Georges Gielen, "Simulation-based optimization of UGCs performances", in Proc. of the 7th IEEE International Caribbean Conference on Devices, Circuits and Systems, pp. 1-4, April 2008.

[C49] [ISQED'08] *Xiaoji Ye, Min Zhao, Rajendran Panda, Peng Li, and Jiang Hu, "Accelerating clock mesh simulation using matrix-level macromodels and dynamic time step rounding," in Proc. of IEEE Int. Symp. on Quality Electronic Design, pp. 627-632, March 2008 (acceptance rate 30%).

[C48] [TAU'08] *Xiaoji Ye, *Wei Dong, and Peng Li, "A multi-algorithm approach to parallel circuit simulation," in Proc. of ACM/IEEE Int. Workshop on Timing Issues in the Specification and Synthesis of Digital Systems, February 2008.

[C47] [ICCAD'07] *Zhuo Feng and Peng Li, "A methodology for timing model characterization for statistical static timing analysis," in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 725-729, November 2007 (acceptance rate 27.3%).

[C46] [ICCAD'07] *Xiaoji Ye, Peng Li, Min Zhao, Rajendran Panda, and Jiang Hu, "Analysis of large clock meshes via harmonic-weighted model order reduction and port sliding," in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 627-631, November 2007 (acceptance rate 27.3%).

[C45] [ICCAD'07] *Wei Dong, *Zhuo Feng, and Peng Li, "Efficient VCO phase macromodel generation considering statistical parametric variations," in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 874-878, November 2007 (acceptance rate 27.3%).

[C44] [ICCAD'07] Yang Yi, Peng Li, Vivek Sarin, and Weiping Shi, "Impedance extraction for 3-D

structures with multiple dielectrics using preconditioned boundary element method", in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 7-10, November 2007 (acceptance rate 27.3%).

[C43] [ICCAD'07]*Guo Yu and Peng Li, "Yield-aware analog integrated circuit optimization using Geostatistics motivated performance modeling," in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 464-469, November 2007, (acceptance rate 27.3%).

[C42] [ITC'07] *Guo Yu and Peng Li, "A methodology for systematic built-in self-test of phase-locked loops targeting at parametric failures," pp. 1-10, in Proc. of IEEE Int. Test Conference, October 2007.

[C41] [BMAS'07] Garng M. Huang, *Wei Dong, Yenpo Ho, and Peng Li, "Tracing SRAM separatrix for dynamic noise margin analysis under device mismatch," in Proc. of IEEE Int. Behavioral Modeling and Simulation Conf., pp. 6-10, September 2007.

[C40] [CICC'07] *Wei Dong, Peng Li, and *Xiaoji Ye, "Efficient frequency-domain simulation of massive clock meshes using parallel harmonic balance," in Proc. of IEEE Custom Integrated Circuits Conference, pp. 631-634, September 2007 (acceptance rate 48.2%).

[C39] [DAC'07] *Xiaoji Ye, Yaping Zhan, and Peng Li, "Statistical leakage power minimization using fast equi-slack shell based optimization," in Proc. of IEEE/ACM Design Automation Conference, pp. 853-858, June 2007 (acceptance rate 23.2%).

[C38] [DAC'07] *Guo Yu, *Wei Dong, *Zhuo Feng, and Peng Li, "A framework for accounting for process model uncertainty in statistical static timing analysis," in Proc. of IEEE/ACM Design Automation Conference, pp. 829-834, June 2007 (acceptance rate 23.2%).

[C37] [DAC'07] *Wei Dong and Peng Li, "Accelerating harmonic balance simulation using efficient parallelizable hierarchical preconditioning," in Proc. of IEEE/ACM Design Automation Conference, pp. 436-439, June 2007 (acceptance rate 23.2%).

[C36] [DAC07] *Zhuo Feng, Peng Li, and Yaping Zhan, "Fast second-order statistical static timing analysis using parameter dimension reduction," in Proc. of IEEE/ACM Design Automation Conference, pp. 244-249, June 2007 (acceptance rate 23.2%).

[C35] [ISQED'07] *Guo Yu, Peng Li, and *Wei Dong, "Achieving low-cost linearity test and diagnosis of Sigma-Delta ADCs via frequency-domain nonlinear analysis and macromodeling", in Proc. of IEEE Int. Symp. on Quality Electronic Design, pp. 513-518, March 2007 (acceptance rate 33%).

[C34] [ISQED'07] *Zhuo Feng, *Guo Yu, and Peng Li, "Reducing the complexity of VLSI performance variation modeling via parameter dimension reduction", in Proc. of IEEE Int. Symp. on Quality Electronic Design, pp. 737-742, March 2007 (acceptance rate 33%).

[C33] [TAU'07] *Xiaoji Ye, Yaping Zhan, and Peng Li, "Statistical leakage power minimization using fast equi-slack shell based optimization," in Proc. of ACM/IEEE Int. Workshop on Timing Issues in the Specification and Synthesis of Digital Systems, pp. 37-42, February 2007 (acceptance rate 44.0%).

[C32] [TAU'07] *Zhuo Feng and Peng Li, "Parameterized waveform-independent gate models for timing and noise analysis", in Proc. of ACM/IEEE Int. Workshop on Timing Issues in the Specification and Synthesis of Digital Systems, pp. 61-65, February 2007 (acceptance rate 44.0%).

[C31] [ICCAD'06] *Zhuo Feng and Peng Li, "Performance-oriented statistical parameter reduction of parameterized systems via reduced rank regression," in Proc. of IEEE/ACM Int. Conf. on Computer-

Aided Design, pp. 868-875, November 2006 (acceptance rate 23.4%)
(**Best paper award nomination, 16 out of 541 submissions, 3%).**

[C30] [ICCAD'06] *Xiaoji Ye, Peng Li, and Frank Liu, "Practical variation-aware interconnect delay and slew analysis for statistical timing verification", in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 54-59, November 2006 (acceptance rate 23.4%).

[C29] [ICCAD'06] Ganesh Venkataraman, *Zhuo Feng, Jiang Hu, and Peng Li, "Combinatorial algorithms for fast clock mesh optimization," in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 563-567, November 2006 (acceptance rate 25.1%).

[C28] [EPEP'06] Yang Yi, Peng Li, Vivek Sarin, and Weiping Shi, "A preconditioned hierarchical algorithm for impedance extraction of interconnects in packages," 15th IEEE Topical Meeting on Electrical Performance of Electronic Packaging (EPEP), pp. 99-102, October, 2006.

[C27] [DAC'06] *Guo Yu and Peng Li, "Lookup table based simulation and statistical modeling of Sigma-Delta ADCs", in Proc. of IEEE/ACM Design Automation Conference, pp.1035-1040, July 2006 (acceptance rate 20.8%).

[C26] [DAC'06] Peng Li and Weiping Shi, "Model order reduction of linear networks with massive ports via frequency-dependent port packing," in Proc. of IEEE/ACM Design Automation Conference, pp. 267-272, July 2006 (acceptance rate 20.8%).

[C25] [DAC'06] Shiyan Hu, Qiuyang Li, Jiang Hu, and Peng Li, "Steiner network construction for timing critical nets," in Proc. of IEEE/ACM Design Automation Conference, pp. 379-384, July 2006 (acceptance rate 20.8%).

[C24] [ISQED'06] *Zhuo Feng, Peng Li, and Jiang Hu, "Efficient model update scheme for general link-insertion networks," in Proc. of IEEE Int. Symp. on Quality Electronic Design, pp. 43-50, March 2006 (acceptance rate 36.3%).

[C23] [ISQED'06] Peng Li, "Critical path analysis considering temperature, power supply variations and temperature induced leakage," in Proc. of IEEE Int. Symp. on Quality Electronic Design, March 2006 (acceptance rate 36.3%).

[C22] [ICCAD'05] Peng Li, "Variational analysis of large power grids by exploring statistical sampling sharing and spatial locality," in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 645-651, November 2005 (acceptance rate 23.7%).

[C21] [ICCAD'05] Xin Li, Peng Li, and Lawrence Pileggi, "Parameterized interconnect order reduction with explicit-and-implicit multi-parameter moment matching for inter/intra-die variations," in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 806-812, November 2005 (acceptance rate 23.7%).

[C20] [ICCAD'05] G. Venkataraman, N. Jayakumar, J. Hu, P. Li, S. Khatri, A. Rajaram, P. McGuinness, and C. Alpert, "Practical techniques to reduce skew and its variations in buffered clock networks," in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 592-596, November 2005 (acceptance rate 23.7%).

[C19] [ICCD'05] Peng Li and Emrah Acar, "A waveform independent gate model for accurate timing analysis," in Proc. of IEEE Int. Conf. on Computer Design, pp. 363-365, October 2005 (acceptance

rate 23.0%).

[C18] [ICCD'05] Peng Li, Yongdong Deng, and Lawrence Pileggi, "Temperature-dependent optimization of cache leakage power dissipation," in Proc. of IEEE Int. Conf. on Computer Design, pp. 7-12, October 2005 (acceptance rate 23.0%).

[C17] [CICC'05] Rohan Batra, Peng Li, Lawrence T. Pileggi, and Wan-ju Chiang, "A behavioral level approach for nonlinear dynamic modeling of voltage-controlled oscillators," in Proc. of IEEE Custom Integrated Circuit Conference, pp. 717-720, September 2005 (acceptance rate 26.3%).

[C16] [DAC'05] Peng Li, "Power grid simulation via efficient sampling-based sensitivity analysis and hierarchical symbolic relaxation," in Proc. of IEEE/ACM Design Automation Conference), pp. 664-669, June 2005 (acceptance rate 21.0%).

[C15] [DATE'05] Peng Li, Frank Liu, Xin Li, Lawrence Pileggi, and Sani Nassif, "Modeling interconnect variability using efficient parametric model order reduction," in Proc. of Design Automation and Test In Europe Conference (DATE), pp. 958-963, March 2005, (acceptance rate 21.3%).

[C14] [DATE'05] Sounil Biswas, Peng Li, Ronald D. Blanton, and Lawrence T. Pileggi, "Specification test compaction for analog circuits and MEMS," in Proc. of Design Automation and Test In Europe Conference (DATE), pp. 164-169 March 2005 (acceptance rate 21.3%).

[C13] [ICCAD'04] Peng Li, Lawrence Pileggi, Mehdi Asheghi, and Rajit Chandra, "Efficient full-chip thermal modeling and analysis," in Proc. of IEEE/ACM Int. Conf. on Computer-Aided Design (ICCAD), pp. 319-326, November 2004 (acceptance rate 24.4%).

[C12] [ICCAD'04] Peng Li and Lawrence Pileggi, "Efficient harmonic balance simulation using multi-level frequency decomposition," in Proc. IEEE/ACM Int. Conf. on Computer-Aided Design (ICCAD), pp. 677-682, November 2004 (acceptance rate 24.4%).

[C11] [BMAS'04] Rohan Batra, Peng Li, Lawrence Pileggi, and Yu-Tsun Chien, "A methodology for analog circuit macromodeling," in Proc. of IEEE International Behavioral Modeling and Simulation Conference, pp. 41- 46, October 2004.

[C10] [DAC'04] Xin Li, Yang Xu, Peng Li, Padmini Gopalakrishnan, and Lawrence Pileggi, "A frequency relaxation approach for analog/RF system-Level simulation," in IEEE/ACM Design Automation Conf. , pp. 842-847, June 2004, (acceptance rate 20.8%).

[C9] [BMAS'03] Peng Li and Lawrence Pileggi, "Modeling nonlinear communication ICs using a multivariate formulation," in Proc. of IEEE International Workshop on Behavioral Modeling and Simulation, pp. 24-27, October 2003.

[C8] [ICCAD'03] Peng Li, Xin Li, Yang Xu, and Lawrence Pileggi, "A hybrid approach to nonlinear macromodel generation for time-varying analog circuits," in Proc. IEEE/ACM Int. Conf. on Computer-Aided Design, pp. 454-461, November 2003 (acceptance rate 26.3%).

[C7] [DAC'03] Peng Li and Lawrence Pileggi, "NORM: compact model order reduction of weakly nonlinear systems," in Proc. of 40th IEEE/ACM Design Automation Conference, pp. 472-477, June 2003, (acceptance rate 24.2%) (**Best Paper Award, four out of 628 submissions, 0.6%**).

[C6] [DAC'03] Xin Li, Peng Li, Yang Xu and Lawrence Pileggi, "Analog and RF circuit macromodels for system-level analysis," in Proc. of 40th IEEE/ACM Design Automation Conference (DAC), pp. 478-483, June 2003, (acceptance rate 24.2%).

[C5] [DATE'03] Yang Xu, Xin Li, Peng Li, and Lawrence Pileggi, "Noise macromodel for radio frequency integrated circuits," in Proc. of IEEE/ACM Design Automation & Test In Europe Conference (DATE), pp. 150-155, March 2003 (acceptance rate 25.8%).

[C4] [ASP-DAC'03] Peng Li and Lawrence Pileggi, "Nonlinear distortion analysis via linear-centric models," in Proc. of IEEE/ACM Asia and South Pacific Design Automation Conf., pp. 897-903, January 2003, (acceptance rate 33.6%).

[C3] [ASP-DAC'03] Xin Li, Peng Li, Yang Xu, Robert Dimaggio and Lawrence Pileggi, "A frequency separation macromodel for system-level simulation of RF circuits," in Proc. of IEEE/ACM Asia and South Pacific Design Automation Conf., pp. 891-896, January, 2003 (acceptance rate 33.6%).

[C2] [DATE'02] Peng Li and Lawrence Pileggi, "A linear-centric approach to harmonic balance analysis," in Proc. of IEEE/ACM Design Automation & Test In Europe Conf., pp. 634-639, March 2002 (acceptance rate 29.8%).

[C1] [SLIP'00] Peng Li, Pranab K. Nag, and Wojciech Maly, "Cost based tradeoff analysis of standard cell designs," in Proc. of ACM International Workshop on System-Level Interconnect Prediction, pp. 129-135, April 2000.

Book Chapters

[B6] Peng Li, *Wei Dong, and Garng M. Huang, "Dynamic stability of static memories: concepts and advanced numerical analysis techniques," 19 pages, in *Simulation and Verification of Electronic and Biological Systems* , Peng Li, L. Miguel Silveira and Peter Feldmann (Eds.), Springer 2011.

[B5] Peng Li and Wei Dong, "Parallel preconditioned hierarchical harmonic balance for analog and RF circuit simulation," pp. 111-130, in *Advances in Analog Circuits*, IN-TECH Press (http://www.intechweb.org), ISBN 978-953-307-323-1, February 2011.

[B4] Esteban Tlelo-Cuautle, Elyoenai Martínez-Romero, Carlos Sánchez-López, Francisco V. Fernández, Sheldon X.-D. Tan, Peng Li, and Mourad Fakhfakh, "Behavioral modeling of mixed-mode integrated circuits," pp.85-108, in *Advances in Analog Circuits*, IN-TECH Press (http://www.intechweb.org), ISBN 978-953-307-323-1, February 2011.

[B3] Rasit Onur Topaloglu, *Zhuo Feng, and Peng Li, "Interconnect variability and performance analysis," pp. 21-39 , in *Recent Topics on Modeling of Semiconductor Processes, Devices and Circuits*, Rasit Onur Topaloglu and Peng Li (Eds.), Bentham Publishing (www.ebook-engineering.org) 2011.

[B2] Rasit Onur Topaloglu, *Guo Yu, and Peng Li, "Probability propagation and yield optimization for analog circuits," pp. 61-80, in *Recent Topics on Modeling of Semiconductor Processes, Devices and Circuits*, Rasit Onur Topaloglu and Peng Li (Eds.), Bentham Publishing (www.ebook-engineering.org) 2011.

[B1] *Guo Yu and Peng Li, "Robust design and test of analog/mixed-signal circuits in deeply scaled CMOS technologies", pp. 453-374, in *VLSI* (book title), IN-TECH Press

(http://www.intechweb.org/), ISBN 978-953-307-049-0, February 2010.

PATENTS

[P3] P. Li, L. Pileggi, M. Asheghi and R. Chandra, Methods and Apparatus for thermal modeling and analysis of semiconductor chip designs, US patent No. 7,401,304 B2, issued in July 2008.

[P2] X. Li, Y. Yu, P. Li and L. Pileggi, Analog and Radio Frequency (RF) System-level Simulation Using Frequency Relaxation, US patent No. 7,653,524 B2, issued in January 2010.

[P1] X. Li, P. Li and L. Pileggi, Method for Parameterized Model Order Reduction of Integrated Circuit Interconnects, US patent No. 7,908,131 B1, issued in March 2011.

ADVISEES

Current Students

Ayaz Abdullah	B.S.	Laisha Prakash	M.S.
Abdullah Alquwayzani	B.S.	Deepika Ravipati	M.S.
Ting-Jui Chang	M.S.	Ashvin Shenoy Renjal	M.S.
Yukun He	M.S.	Myung Seok Shim	Ph.D.
Zong-Fu Hsieh	Ph.D.	Sai Sourabh Yenamachintala	M.S.
Hanbin Hu	Ph.D.	Yu Wang	M.S.
Jeonjun Lee	Ph.D.	Xin Zhan	Ph.D.
Suil Lee	B.S.	Wenrui Zhang	Ph.D.
Yang Li	M.S.	Renqian Zhang	M.S.
Yu Liu	Ph.D.	Chenye Zhao	M.S.

Graduated Doctoral Students

15. Yingyezhe (Jimmy) Jin	Ph.D., August 2018
Thesis title:	"Architectures and Training Algorithms of Deep Spiking Neural Networks"
First employment:	Research Engineer, Facebook, Bay area, California
14. Ya (Tony) Wang	Ph.D., December 2017
Thesis title:	"Efficient and Robust Simulation, Modeling and Characterization of IC Power Delivery Circuits"
First employment:	Google, Bay area, California
13. Honghuang Lin	Ph. D., August 2016
Thesis title:	"Algorithms for Verification of Analog and Mixed-Signal Integrated Circuits"
Current employment:	Apple, Bay area, California

12. Qian Wang	Ph. D., August 2016
Thesis title:	"Architectures and Design of VLSI Machine Learning Systems"
Current employment:	Computer Vision Research Engineer, Apple, Santa Clara, California
11. Parijat Mukherjee	Ph. D., December 2014
Thesis title:	"Detection and Diagnosis of Out-of-Specification Failures in Mixed-Signal Circuits"
First employment:	Strategic CAD Laboratories, Intel Corporation, Hillsboro, Oregon
10. Tong Xu	Ph. D., December 2014
Thesis title:	"Circuit and System Level Design Optimization for Power Delivery and Management"
First employment:	Cadence Design Systems, San Jose, California
9. Suming Lai	Ph. D., December 2014 (defended in November 2013)
Thesis title:	"Modeling, Design and Optimization of IC Power Delivery with On-chip Voltage Regulation"
First employment:	Maxim, San Diego, California
8. Yong Zhang	Ph. D., May 2014 (defended in December 2013)
Thesis title:	"Simulation and Design of Biological and Biologically-Motivated Computing Systems"
First employment:	Cadence Design Systems, San Jose, California
7. Yongtae Kim	Ph. D., December 2013
Thesis title:	"Energy Efficient and Error Resilient Neuromorphic Computing in VLSI"
Current position:	Assistant Professor, Kyungpook National University, Korea
Previous employment:	Intel Corporation, Santa Clara, California
6. Leyi Yin	Ph. D., December 2012
Thesis title:	"Formal Verification and In-Situ Test of Analog and Mixed-Signal Circuits"
First employment:	Cirrus Logic, Austin, Texas
5. Zhiyu (Albert) Zeng	Ph.D., December 2011
Thesis title:	"Scalable Analysis, Verification and Design of IC Power Delivery"
First employment:	Samsung Austin Research Center (SARC), Austin, Texas (now with Cadence Design Systems, Austin, Texas)
4. Xiaoji Ye	Ph.D., December 2010 (defended in July 2010)
Thesis title:	"Parallel VLSI Circuit Analysis and Optimization"
First employment:	Intel Corporation, Hillsboro, Oregon

3. Guo Yu	Ph.D., December 2009
Thesis title:	"Modeling, Test and Optimization of Robust Analog and Mixed-Signal ICs"
First employment:	Oracle Corporation, Austin, Texas
2. Zhuo Feng	Ph.D. August 2009
Thesis title:	"Modeling, Analysis and Verification of Large-Scale On-Chip Interconnect"
Employment:	Associate Professor (NSF Career Award Recipient), Michigan Technological University, Houghton, Michigan
1. Wei Dong	Ph.D., August 2009
Thesis title:	"Parallel Algorithms for Time and Frequency Domain Circuit Simulation"
First employment:	Texas Instruments, Dallas, Texas

Former Post-Doctoral Fellow

Boyuan Yan	Post-Doc**,** March 2010 – August 2012
Current Position:	Assistant Professor of Research Cornell Medical College/Cornell University

Graduated Master's Students with Thesis and Defense

28. Ting-Jui Chang	M.S., December 2018
Thesis title:	"Enhancing resilience against adversarial attacks of deep neural networks using efficient two-step adversarial defense"
27. Yukun He	M.S., December 2018
Thesis title:	"Robust Dynamic Step Adversarial Training Defense for Deep Neural Networks"
26. Amarnath Mahadevuni	M.S., May 2018
Thesis title:	"Autonomous Navigation using Reinforcement Learning with Spiking Neural Networks"
First employment:	Nvidia, Durham, NC
25. Qingran Zheng	M.S., December 2017
Thesis title:	"Hybrid Verification for Analog and Mixed-Signal Circuits"
First employment:	Synopsys, Mountain View, California
24. Sushirdeep Narayana	M.S., May 2017
Thesis title:	"Affect Recognition using Electroencephalography Features"
Position after graduation:	Ph.D. student, UIC

23. Seungjai Ahn	M.S., May 2017
Thesis title:	"Energy-efficient Q-learning for collision avoidance of autonomous robots"
First Employment:	Intelligent Safety Research Team, Hyundai, Uiwang, Korea
22. Youjie Li	M.S., May 2016
Thesis title:	"Energy efficient spiking neuromorphic architectures for pattern recognition"
First Employment:	Ph. D. student in ECE, UIUC
21. Ang Li	M.S., August 2016
Thesis title:	"Noise-sensitive loop identification for linear time-varying analog circuits"
First Employment:	Analog Devices, Greensboro, NC
20. Sai Srujan Gudibandi	M.S., August 2016
Thesis title:	"PPG heart rate detection in the presence of motion artifacts"
First Employment:	Global Prior Art Inc., Boston, MA
19. Yen-Ju Lin	M.S., August 2016
Thesis title:	"FPGA-based cascade support vector machine with integrated training"
18. Hariharan Bhagavatheeswaran	M.S., December 2015
Thesis title:	"Hardware accelerator for HMM based speech recognition"
First Employment:	Qualcomm, San Jose, California
17. Di Gao	M.S., December 2015
Thesis title:	"Multi-harmonic modeling of low-power PWM DC-DC converters"
First Employment:	Cadence Design Systems, San Jose, California
16. Kumaran Thulasiraman	M.S., August 2015
Thesis title:	"Enhanced reinforcement learning with attentional feedback and temporally attenuated distal rewards"
First Employment:	Cisco, San Jose, California
15. David Fan	M.S., May 2015
Thesis title:	"Backpropagation for continuous theta neuron networks"
First Employment:	Ph. D. student in ECE, Georgia Institute of Technology
14. Nityendra Singh	M.S., December 2014
Thesis title:	"Training algorithms for networks of spiking neurons"
First Employment:	Cadence Design Systems, San Jose, California

13. Botang Shao	M.S., August 2014
Thesis title:	"Design of Energy-Efficient Approximate Arithmetic Circuits"
First Employment:	Freescale Semiconductor, Austin, Texas
12. Shaoda James Yu	M.S., August 2014
Thesis title:	"EEG-based Drowsiness Detection using Support Vector Machine"
First Employment:	BioTex, Inc., Houston, Texas
11. Ahmad Bashaireh	M.S., May 2014
Thesis title:	"Design Robustness Analysis of Neuromorphic Circuits" Continued as Ph. D. student in Power Systems/Electronics at TAMU
10. Ruicheng Dai	M.S., August 2012
Thesis title:	"Parallel and Distributed Multi-Algorithm Circuit Simulation"
First Employment:	Nvidia, Santa Clara, California
9. Yue Deng	M.S. May 2012
Thesis title:	"SAT-based Verification for Analog and Mixed-Signal Circuits"
First Employment:	Zipalog, Plano, Texas
8. Jingzhen Hu	M.S., May 2012
Thesis title:	"Biophysically accurate Brain Modeling and Simulation Using Hybrid MPI/OpenMP Parallel Processing"
First Employment:	Advanced Micro Devices(AMD), Sunnyvale, California
7. Mingchao Wang	M.S., May 2012
Thesis title:	"Large-scale Simulation of Neural Networks with Biophysically Accurate Models on Graphics Processors"
First Employment:	Mentor Graphics, Wilsonville, Oregon
6. Amandeep Singh	M.S., May 2011
Thesis title:	"Behavioral Model Equivalence Checking for Large Analog/Mixed Signal Systems"
First Employment:	Cypress Semiconductors, San Jose, California
5. Parijat Mukherjee	M.S., December 2010
Thesis title:	"Automatic Stability Checking for Large Linear Analog Circuits" Pursued Ph.D. in the same group
4. Srinath Narasimhan	M.S., May 2010
Thesis title:	"Circuit Optimization Using Efficient Parallel Pattern Search"
First employment:	Intel Corp., Hillsboro, Oregon

3. Akshit Dayal	M.S., December 2009
Thesis title:	"Robust Optimization of Nanometer SRAM Designs"
First employment:	Texas Instruments, Houston, Texas
2. Chang Zhao	M.S., December 2009
Thesis title:	"Statistical Performance Modeling of SRAMs"
First employment:	Precision Reservoir Modeling Inc., Houston, Texas (Currently with Synopsys, Hillsboro, Oregon)
1. Xiaoji Ye	M.S., August 2007
Thesis title:	"Fast High-Order Variation-Aware IC Interconnect Analysis" Pursued Ph.D. in the same group

PROFESSIONAL ACTIVITIES

Vice President for Technical Activities, IEEE Council of Electronic Design Automation, Jan. 2016 – Dec. 2017

Editorial board, Journal of Low Power Electronics (JOLPE), 2008 – Present

Associate Editor, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2008 – 2013

Associate Editor, IEEE Trans. on Circuits and Systems II (TCAS2), 2008 – 2016

Panel Co-Chair, 2019
Technical Program Committee Member, 2007 – 2009
EEE Int. Symposium on Quality Electronic Design (ISQED)

Co-Chair of EDA track, Technical Program Committee, 2017
IEEE International Conference on Computer Design (ICCD)

Technical Program Committee Member, 2017, 2018
IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)

General Chair, 2010
Technical Program Committee Chair, 2009
Technical Program Committee Member, 2007-2009, 2013, 2015, 2016, 2017, 2018, 2019
ACM/IEEE Workshop on Timing Issues in the Specification and Synthesis of Digital Systems

Subcommittee TPC Chair, Timing Analysis, Integrity and Design Reliability, 2011, 2012
Technical Program Committee Member, 2010, 2011, 2012, 2018, 2019
IEEE/ACM Design Automation Conference (DAC)

Technical Program Committee Member, 2006-2009, 2014, 2015, 2017

Subcommittee TPC Chair, Analog Mixed-signal, RF/Mixed-Domain Simulation (Device Models), 2008-2009, IEEE/ACM Int. Conf. on Computer-Aided Design (ICCAD)

Co-organizer, DAC Workshop on Autonomous Vehicles, Avionics, Transportation, and Robotics (AVATAR), June 2017

Co-organizer, ACM/IEEE Early Career Workshop at DAC, June 2017

Technical Program Committee Member, 2015, 2016, 2017
International Joint Conference on Neural Networks (IJCNN)

Co-organizer, June 5, 2016
ACM/IEEE DAC Workshop on Internet of Things (IoT)
Austin, TX

Co-organizer, June 5, 2016
IEEE CEDA Career Perspectives Panel
Collocated with ACM/IEEE Design Automation Conference
Austin, TX

ACM Student Research Competition at ICCAD
Technical Program Committee Member, 2016

Technical Program Committee Member, Frontiers in Analog CAD (FAC) Workshop, 2011, 2013, 2014, 2015, 2017

Book Editor
Simulation and Verification of Electronic and Biological Systems (Li, Silveira, Feldmann Eds.), Publisher: Springer, 2011, with 22 contributors from Boehringer Ingelheim Pharmaceuticals, Designer's Guide Consulting, Goethe University of Frankfurt, MIT, Sandia National Laboratories, Synopsys, Texas A&M U., Texas Instruments, UC Berkeley, UC Davis, UCSF

Guest Editor
"Special Section PAR-CAD: Parallel CAD Algorithms and CAD for Parallel Architectures/Systems," 2011
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems

Book Editor
Recent Topics on Modeling of Semiconductor Processes, Devices and Circuits (Eds. Topaloglu, Li), Publisher: Bentham Publishing, 2011, with 18 contributors from Arizona State U., GLOBALFOUNDRIES, IBM, Michigan Tech., National Taiwan U., Nanyang Technological U., Oracle, Texas A&M U., Texas Instruments, UCLA, UC Riverside, U. Wisconsin.

Guest Editor
"Special Section Parallel CAD: Algorithm Design and Programming," 2010.
ACM Transactions on Design Automation of Electronic Systems (TODAES)

ACM SIGDA Physical Design Technical Committee, 2009

Technical Activities Committee, IEEE CEDA (Council on Electronic Design Automation), 2009

Co-organizer, Circuit and Multi-Domain Simulation Workshop (CMS), co-located with ICCAD, 2009

Best Paper Award Selection Committee, IEEE/ACM Int. Conf. on Computer-Aided Design (ICCAD), 2009

Selection Committee, The ACM Outstanding Ph.D. Dissertation Award in Electronic Design Automation, 2006

Review Committee Member, IEEE Int. Symp. on Circuits & Systems (ISCAS), 2005 – 2009

Committee Member, Ph.D. Forum, IEEE/ACM Design Automation Conference (DAC), 2005 – 2009.

NSF Proposal Review Panels
ECCS/Engineering, CCF/CISE, SBIR/STTR: 2009, 2010, 2012, 2016, 2017, 2018

External Reviewer, Hong Kong Research Grants Council, 2013

Reviewer for Journals:

- IEEE Transactions on Computer-Aided Design
- IEEE Transactions on Circuits and Systems, I
- IEEE Transactions on Circuits and Systems, II
- IEEE Transactions on VLSI
- IEEE Design and Test of Computers
- IEEE Transactions on Nanotechnology
- IEEE Transactions on Power Electronics
- IEEE Transactions on Neural Networks and Learning Systems
- IEEE Transactions on Semiconductor Manufacturing
- IEEE Journal on Emerging and Selected Topics in Circuits and Systems
- ACM Transactions on Design Automation of Electronic Systems
- ACM Journal on Emerging Technologies in Computing Systems
- Neural Networks
- Springer Journal of Analog Integrated Circuits and Signal Processing
- Springer Journal of Optimization and Engineering
- Foundations and Trends in Electronic Design Automation
- Integration, the VLSI Journal
- Journal of Computational Neuroscience
- VLSI Design, Hindawi
- Computational Intelligence and Neuroscience, Hindawi
- Journal of Low Power Electronics (JOLPE)
- Journal of Microprocessors and Microsystems, Elsevier

IET Circuits, Devices & Systems

Reviewer for Conferences (selected):
IEEE/ACM International Conference on Computer-Aided Design (ICCAD)
IEEE/ACM Design Automation Conference (DAC)
IEEE International Symposium on Circuits & Systems (ISCAS)
International Joint Conference on Neural Networks (IJCNN)
IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)
IEEE International Symposium on Quality Electronic Design (ISQED)
IEEE International SOC Conference
ACM International Symposium on Physical Design (ISPED)
IEEE Biomedical Circuits & Systems Conference (BioCAS)
ACM/IEEE Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)
Frontiers in Analog CAD (FAC) Workshop
IEEE/ACM Design, Automation and Test in Europe (DATE)

Reviewer for Book Publishers:
John Wiley & Sons
Cambridge University Press

Memberships: Fellow of the IEEE, Member of the ACM, Member of AAAS

DEPARTMENTAL SERVICE

ECE Faculty Advisory Committee (FAC):
Member, 9/1/2016 – 8/31/2018; Chair, 9/1/2017 – 8/31/2018

Tenure & Promotion Committee: member, 9/1/2018 – 8/31/2019

Staff and Faculty Internal Awards Committee: member, 9/1/2018 – 8/31/2019

Graduate Studies Committee: member, 9/1/2018 – 8/31/2019

Faculty Recruitment and Hiring Committee, 9/1/2015 – 8/31/2017

Graduate Recruitment, Admission, Fellowships, and Scholarships Committee, 2014 – 2018

Teaching Load Committee, June 2016 – July 2016

Computer Engineering Curriculum Coordination Committee, 2013 –

Reviewer of Computer Engineering Graduate Applications, Fall 2009 –

ECE Graduate Studies Committee, Fall 2010

SELECTED INVITED SEMINARS

"Rare Failure Detection of Analog and Mixed-Signal Circuits: A Statistical Machine Learning

Approach"
Semiconductor Research Corporation (SRC) e-Workshop
Texas Analog Center of Excellence (TxACE), University of Texas, Dallas, September 2018

"Enabling Verification of Analog and Mixed-Signal Circuits using Machine Learning"
SRC/NSF Verification, Validation, and Test of Machine Learning Systems (V-TML) Workshop
Alexandria, VA, July 2018

"Recurrent Spiking Neural Networks: Models & Hardware Design"
Xidian University, Xi'an, China, June 2018

"From Statistics to Spiking Neurons: Algorithms, Architectures, and Circuits for IC Design Verification and Neuromorphic Computing"
University of California, Santa Barbara, May 2018

"Spiking Neural Networks: Learning Mechanisms and Hardware Implementation"
Semiconductor Research Corporation (SRC) e-Workshop, December 2017

"Biologically-Plausible Spiking Neural Networks: Modeling and Computation"
Institute of Artificial Intelligence and Robotics, Xi'an Jiaotong University, Xi'an, China, July 2017

"Verification and Test of Analog/Mixed-Signal Circuits – A Machine Learning Approach"
Shanghai Jiao Tong University, Shanghai, China, July 2017

"Verification and Test of Analog/Mixed-Signal Circuits – A Machine Learning Approach"
Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan, July 2017

"Research Overview on Machine Learning"
Automotive Products Research Laboratory (APL), Hitachi, Farmington Hills, MI, June 2017

"An Architecture for On-chip Self-Adaptive Reservoir Computing"
Institute of Neuroinformatics, University of Zurich and ETH Zurich, Zurich, Switzerland, March 2017

"Hardware Architecture for Computing with Recurrent Spiking Neural Networks"
University of Maryland, College Park, MD, October 2016
"Sparse Bayesian Learning for Verification and Test of Analog/Mixed-Signal Circuits"
Semiconductor Research Corporation (SRC) e-Workshop, July 2016

"Enabling Distributed On-Chip Voltage Regulation: Stability Assurance and Performance Optimization"
Xidian University, Xi'an, China, June 2016

"Computation with Recurrent Spiking Neural Networks in VLSI"
McGill University, Montreal, Canada, May 2016

"Simulation and Macromodeling of DC-DC Converters"
Texas Analog Center of Excellence (TxAcE), University of Texas, Dallas, July 2015

"Advanced Design Automation Methodologies for Next-Generation Power Delivery Networks"
Tutorial at IEEE/ACM Design Automation Conference, San Francisco, CA, June 2015
Organizer and Presenter with Zhuo Feng (Michigan Technological Univ.), Cheng Zhuo (Intel) and Karthikeyan Ramamurthi (Intel)

"Biophysically based Computational Simulation of Oscillatory Activities of the Brain"
Pierre and Marie Curie University (UPMC), Paris, France, March 2015

"Computational Modeling and Simulation of Synchronized Firing Behaviors of the Brain"
Invited talk at Design, Automation and Test in Europe Conference (DATE), March 2015

"Holistic Design of IC Power Delivery: Design Tradeoffs and System Optimization"
Shanghai Jiao Tong University, Shanghai, China, July 2014

"Biophysically based Computational Simulation of Oscillatory Activities of the Brains"
East China Normal University, Shanghai, China, July 2014

"The Theory and Practice of Stability-Ensuring Design of IC Power Delivery with Distributed Voltage Regulators"
Xi'an Jiaotong University, Xi'an, China, July 2014

"Analysis of Oscillatory Behaviors of the Brain"
DAC Workshop- They are all Networks! Analysis and Optimization for Electronics, Water, Electricity, Bio, IEEE/ACM Design Automation Conference (DAC), Austin, Texas, June 2013

"Hierarchical Model Checking for Practical Analog/Mixed-Signal Design Verification"
Freescale Semiconductors SRC Verification E-Forum, March 2013

"Design Analysis of IC Power Delivery"
ICCAD-2012 Special Session: Power Grid Simulation and Verification for Billion-Transistor VLSI Designs
IEEE/ACM Intl. Conf. on CAD (ICCAD), San Jose, California, November 2012
"System Design and Analysis of IC Power Delivery"
Fudan University, Shanghai, China, Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China, and Xi'an Jiaotong University, Xi'an, China, August, 2012

"Design and Analysis of IC Power Delivery with On-Chip Voltage Regulation"
International Conference on IC Design and Technology, Austin, Texas, May 2012

"Circuit/System Co-Optimization of IC Power Delivery"
Advanced Micro Devices (AMD), Austin, Texas, May 2012

"System-Level Modeling and Design of IC Power Delivery"
Freescale Semiconductors, Austin, Texas, May 2012

"Property Checking and Design Assurance for Analog Circuits and Networks"
Strategic CAD Lab, Intel Corporation, Hillsboro, OR, December 2011

"Leveraging GPU Computing for VLSI CAD and Beyond"

CANDE Workshop, San Jose, California, November 2011

"Design and Analysis of Power Delivery Networks with Voltage Regulation and Conversion" Intel Corporation, Hillsboro, OR, June 2011

"Exploiting Parallelism for CAD: Algorithm Design and Implementation Strategies"
DAC PAPA Workshop, San Diego, CA, June 2011

"DAC Parallel EDA Panel"
IEEE/ACM Design Automation Conference, San Diego, CA, June 2011

"From Integrated Circuit Design to Brain Modeling: Coping with System Complexity by Leveraging Application-Specific Parallel Computing"
Ming Hsieh Department of Electrical Engineering,
University of Southern California, Los Angeles, California, March 2011

"In-Situ Jitter Test and Diagnosis"
IBM T. J. Watson Research Center, E-Seminar, NY, December 2010

"Analog Verification: Challenges and Perspectives"
Intel Analog and Mixed-Signal CAD Workshop, Hillsboro, OR, July 2010

"Parallel Circuit Simulation: Algorithms and Runtime Optimization"
SRC/Texas Analog Center of Excellence, Dallas, TX, June 2010.

"CAD Techniques for Large-Scale Circuit Simulation and Design Verification"
Texas Instruments, Dallas, TX, February 2010

"Design and Verification of Power Delivery Networks"
IBM Austin Research Laboratories, Austin, TX, January 2010

"Parallel VLSI CAD: Exploring Parallelisms on Multi-core and Graphics Processors"
IBM T. J. Watson Research Center, Yorktown Heights, NY, May 2009
Tsinghua University, Xi'an Jiaotong University and Fudan University, China, June 2009

"Parallel Preconditioned Harmonic Balance for Analog Circuit Analysis" (invited)
SIAM Conference on Computational Science and Engineering, Miami, FL, March 2009

"Parallel Transient Simulation on Multicore Shared-Memory Machines"
Distinguished Speaker Seminar
IEEE Council on Electronic Design Automation (CEDA), Cadence Research Laboratories, Berkeley, CA, November 2008

"Parallel Circuit Simulation on Multi-core and GPU Platforms"
Intel Strategic CAD Lab, Hillsboro, OR, November 2008

"Novel CAD Techniques for Analyzing SRAM Dynamic Stability and Large Power Grids"
Advanced Micro Devices (AMD), Sunnyvale, CA, November 2008

"CAD for Analog: Variability, Modeling and Optimization"
Cadence Design Systems, Pittsburgh, PA, April 2008

"Model Order Reduction of Parameterized Multi-Port Passive Networks for On-Chip Interconnect Design"
Department of Mathematics, University of Texas, Arlington, TX, April 2008

"Techniques for Parallel Circuit Simulation and SRAM Dynamic Stability Analysis"
IBM Austin Research Lab, Austin, TX, January 2008

"Modeling and Analysis of Non-Tree Clock Distribution"
Cadence Design Systems, San Jose, CA, November 2007

"Recent Results in RF Simulation and Macromodeling"
Texas Instruments, Dallas, TX, July 2007

"Efficient Analog Circuit Analysis Using Hierarchically Preconditioned Harmonic Balance"
Magma Design Automation, Austin, TX, January 2007

"Coping with Complexity: Interconnect Variation Analysis and Simulation of Large Analog and Clock Networks"
Freescale Semiconductors, Austin, TX, November 2006
"Modeling and Analysis of Circuit Performance under Environmental and Process Variations"
Intel Corporation, Austin, TX, May 2006

"Analyzing Circuit Performance under Process, Temperature and Supply Variations"
IBM Austin Research Lab, Austin, TX, March 2006

"Efficient Circuit Delay Analysis Considering Process, Temperature and Supply Variations"
Mentor Graphics Corporation, Wilsonville, OR, March 2006

"Fast Circuit Performance Evaluation in the Presence of Process, Temperature and Supply Variations"
Synopsys, Mountain View, CA, Feb 2006

"Full-Chip Thermal Modeling and Analysis"
Intel Corporation, Santa Clara, CA, April 2005

"Hierarchical Approaches in Circuit Simulation"
Shanghai Jiao Tong University, Fudan University, Xi'an Jiaotong University, China
December 2004 – January 2005

"Nonlinear Reduced-Order Modeling for Analog and RF: Challenges and Opportunities"
University of Illinois at Urbana-Champaign, Yale University, March 2004
Texas A&M University, April 2004.

CONSULTING

Intel Corporation and two silicon-valley startup companies